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# A DUAL CHANNEL INFRARED SCANNER FOR ATMOSPHERIC IMAGING STUDIES AT 10.6 MICRONS

The Ohio State University

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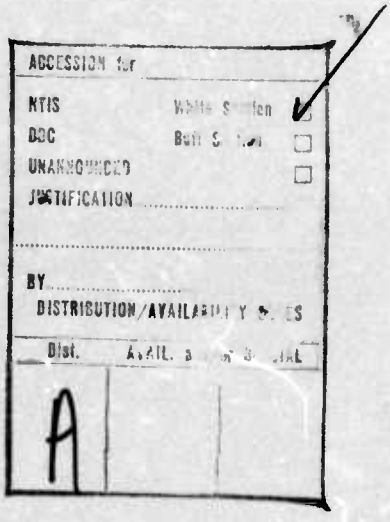


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# A DUAL CHANNEL INFRARED SCANNER FOR ATMOSPHERIC IMAGING STUDIES AT 10.6 MICRONS

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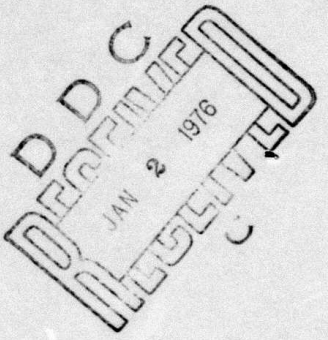




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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A dual channel infrared scanning, display, and recording system originally developed for experiments in atmospheric imaging and image restoration at 10.6 microns has been modified for use with extended targets. Two image formats are now available, one providing two spatially separable images having 40 x 40 element resolution at 200 frames per second and the other, two images having 64 x 64 element resolution at 60 frames per second which may be joined, if desired, to scan a single rectangular image. Visual CRT displays of the

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infrared images are provided and magnetic tape recordings are made which may be played back later at recording speed or at reduced speed for viewing and to provide computer input for data analysis. This report describes in detail the modifications made to the scanning, display, and recording system and, together with the original report published previously, provides complete documentation for the system.

A separate playback, display, and computer interface system, compatible with the scanner system, to be used for image restoration processing has also been developed. Both systems are to be delivered to RADC for infrared imaging and image restoration studies.

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# I. INTRODUCTION

This report which is the final technical report on Contract F30602-73-C-0199 documents the modifications made to the dual-channel infrared scanning, display, and recording system originally developed under Contract F30602-70-C-0003 as described and documented in a previous technical report[1]. The OSU playback and computer interface system required for computer analysis of the recorded data as described briefly in a previous technical report[2] has also been modified to retain compatibility with the IR scanning and recording system. Details of the interface system (not specifically covered by the current contract) are being supplied to RADC under separate cover, together with the associated equipment. Software for system operation and image restoration has been delivered separately.

Briefly, the original system was developed to record, in digital format, two 10.6 micron images simultaneously at 200 frames per second with a resolution of 40 x 40 elements per frame for use in isoplanic patch size and image restoration experiments. This system has now been modified to scan two simultaneous images with a resolution of 64 x 64 elements per frame at 60 frames per second and has provisions for optically joining the two images to provide a single image format of 64 x 128 elements for higher resolution imaging of extended targets.

System modifications include a new scanner sub-assembly (containing motor, scanning disc, sync projectors and detectors, and IR detector mounts), 15 new circuit boards, and an optical prism to replace the image separator of the original system. The original scanning format may be restored, as desired, by inter-changing the scanner sub-assemblies. The new circuit boards are compatible with both the old and new formats which are switch selectable. Additional changes incorporated into the system to facilitate accurate data recording and subsequent playback and analysis include a digital DC restorer with selectable time constant in each video channel to minimize the effects of baseline drift, and simultaneous (rather than independent) recording of A and B channel data points to simplify timing requirements for computer loading of the data during playback.

Chapter II contains a general description and specifications for the modified system, Chapter III contains installation and operating instructions, and Chapter IV presents information on the theory of operation of the various circuts. Chapter V is a summary. Schematic diagrams for the modified system including the new circuit boards are given in Appendix I, Appendix II gives alignment and maintenance information, and Appendix III gives instructions for interchanging the scanner sub-assemblies.

Since the IR imaging system in many respects remains much the same as previously documented, the general intent of this report is to supplement the original report (Ref. 1) by presenting the changes made rather

than to replace it. Consequently, the original report should be retained for reference, and is referred to frequently throughout this report.

## II. DESCRIPTION AND SPECIFICATIONS

The system description and specifications were previously given in Ref. 1, Chapter II. These remain valid except for the changes given below to incorporate the new scanning format.

### A. Scanning Detector Specifications

Specifications for the new scanning format, to be added to the original specifications of Ref. 1, Table I, are given in Table I.

TABLE I

SCANNING DETECTOR SPECIFICATIONS
(Modified Image Format)

| | |
|---|---|
| Frame Rate | 60 frames/sec |
| Resolution | 64 x 64 elements |
| Scanning Aperture Dia. | 0.125 mm |
| Rotation Speed | 3600 RPM |
| Power Requirements: | |
| Scanner Unit | 120v., 60 Hz, 1 Phase, 10 amps max, and 120/208v., 60 Hz, 3 Phase, 3 amps. |

The system signal to noise ratio for a given power input is also reduced by approximately 4 dB because of the decreased size of the scanning aperture.

### B. Scanner System

A general description of the dual channel infrared scanner system has been given previously in Ref. 1, Chapter II. Changes made to the original system are now described.

In order to provide a scanning format of 128 x 64 elements per frame with minimum changes to the original system, the image is split into two halves of 64 x 64 elements each for scanning via the A and B

channels of the dual channel system. In principle, this splitting of a single incident image could be done with the original system by setting the movable corner reflectors (see Fig. 3, Ref. 1) together at the center of the image plane. However, because of imperfections at the sharp edges of the corner reflectors (of no consequence for the original dual image system) degradation and loss of image elements at the center of the field would occur. The inside halves of both corner reflectors have therefore been removed and replaced by a 90° corner prism. The outside halves remain, mounted on the translation stages with stepping motor drive as before, but the stages have been locked into proper position for image splitting and the associated stepping motor drives have been disabled.

The new scanner sub-assembly for the 64 x 64 element format (each channel) is basically the same as before. However, motor speed, disc format, and sync reticles are different. The sync projectors have been modified also to provide greater illumination which is required because of the smaller scanning apertures, and two-axis translation-type infrared detector mounts have been added, together with detector mounted framing masks, to facilitate detector positioning and framing adjustments for the smaller line spacing.

The new scanning disc has 64 scanning apertures with equal angular spacing arranged in two spirals and scans one image frame for each channel, interlaced two-to-one, for each rotation of the disc. The odd-numbered lines for channel A and the even-numbered lines for channel B are scanned during the first half of the disc rotation, followed by the remaining lines during the next half rotation of the disc. Rotation speed is 3600 RPM so that the scanning rate is 60 frames per second. The disc size and image size and shape are the same as before (see Fig. 5, Ref. 1). However, since there are now only 64 scanning apertures rather than 80 as used in the original system, there is more "dead space" between image lines. Part of this additional dead space is used to obtain a dark space sample point for the DC restorer clamp circuit as described later in this section, and in Chapter IV paragraph C-4.

Word, line and frame sync are generated as before using projected reticles and photomultiplier detectors in conjunction with the scanning apertures (for word and line sync) and one extra aperture (for frame sync). Two 32-line reticles are used to obtain word sync in the manner previously described (Ref. 1, Chapter II-A), while a 3-line reticle is used for line and frame sync. The new line sync reticle consists of two line segments, offset to give a uniform time delay between line sync and the first word sync pulse for all raster lines, and the third line segment is used to generate frame sync. Disc sync is not required since there is only one image scanned, and hence only one frame sync pulse, for each rotation of the disc.

Digital DC restorers have been added to the channel A and channel B video circuits prior to the low-pass filters (see Ref. 1, Chapter II-B), to minimize the effects of baseline drift which would otherwise occur

due to the AC coupling required from the IR detectors. Basically, these circuits determine the average dc baseline offset by counting the number of sample points above (up count) and below (down count) the zero level, and then apply a voltage proportional to this difference to the inverting input of a unity gain video amplifier to reduce the offset. Thus the average dc level of the video signal is held near zero. The effective time constant of the circuit may be selected (fast, medium, or slow) by varying the number of counter stages, and hence the gain, of the digital feedback circuit.

The DC restorer circuit may also be operated in the clamp mode if desired. In this mode, a sample point is measured, with the feedback voltage set to zero, during the dark time between successive raster lines. This value is then applied as negative feedback during the scanning of the next raster line effectively clamping the video output, with no IR input, to the lower edge of the signal input range. The clamp mode thus provides the greatest theoretical dynamic range for various signal conditions. However, since only a single sample point is taken to set the dc level for each line, this mode is very succeptable to noise and is useful only when sufficient signal is available to yield a very high signal to noise ratio.

For the new scanning format, (64 x 64 elements per frame at 60 frames per second) the recorded data density is reduced from the former value of 22.6 K bits per inch of magnetic tape to 19.08 K bits per inch. Since the recording system was essentially used at maximum capacity this rather modest reduction in recording density results in a significant reduction in error rate so that adjustment and operation of the recording system is far less critical for the new scanning format.

The original system included capability for a slow speed playback to permit more detailed study of the recorded data. However, since a constant width unblanking pulse was used for each data point at recording speed (120 ips) and for slow speed playback (15 ips) the images displayed during low speed playback appeared rather dim. In the modified system a wider unblanking gate is used (automatically selected) during low speed playback so that image brightness is now essentially independent of playback speed.

## III. INSTALLATION AND OPERATING PROCEDURE

### A. Installation

The installation instructions given in Ref. 1 Chapter III-A are applicable with the following exception: The scanner motor for the new scanner sub-assembly requires 60 Hz 3-phase power rather than 400 Hz. Consequently, the 3-phase power cable (J18) must be connected to a 120/208 volt, 60 Hz, 3 phase supply capable of supplying 3 amperes when this sub-assembly is used. The direction of disc rotation must be checked after initial connection to the power source as described

in Ref. 1. (Because of the change in frequency the 400 cycle power ON buttons mentioned in Ref. 1 have been relabled SCANNER MOTOR ON.)

B. Operation

1. Controls and indicators

Controls for the video DC restorers have been added to the front panel of the console unit (see Fig. 1). These are listed in Table II and should be added to Table II of Ref. 1 which is then applicable to the present system.

TABLE II

SYSTEM OPERATING CONTROLS AND INDICATORS
(Modified System)

| Control or Indicator | Function |
|---|---|
| Channel A and Channel B DC RESTORER | Selects CLAMP mode, or SLOW, MED., or FAST time constant for the corresponding A or B channel video DC restorer |
| Stepping motor selectors: TRANS. A TRANS. B | Inoperative when the image splitting prism is installed |

Note also (Table II) that the translation A and B stepping motor controles are not used when the image splitting prism is installed (see Chapter II), and that the 400 ∿ power ON/OFF controls (Table II of Ref. 1) have been relabled as SCANNER MOTOR ON/OFF.

The image format selector switches should be added to Table III of Ref. 1 (Auxiliary controls and indicators) as shown in Table III, below.

TABLE III

AUXILLIARY CONTROLS AND INDICATORS
(Modified System)

| Unit | Control or Indicator | Normal Setting | Function |
|---|---|---|---|
| Console Control Unit (CU-1) | Image Format | 64 x 64 - when* scanner sub-assembly ISS-2 is in use | Selects proper logic circuits for the scanning and display format in use |
| Scanner | Image Format | 40 x 40 - when scanner sub-assembly ISS-1 is in use | |

*Note: A pre-recorded tape of either format may be played back and displayed by setting the IMAGE FORMAT switch on the Console Control Unit (top of chassis near the right rear corner) to the appropriate position regardless of which scanner sub-assembly is installed.

Other information given in Tables III and IV of Ref. 1 remain valid.

2. Operating procedure

The operating procedure given in Ref. 1, Chapter III-B-2 should be followed keeping in mind the change in notation of the "400 ∿ power" controls to "scanner motor" controls and the fact that the image positioning controls (TRANS. A and TRANS. B) are inoperative when the image splitting prism is installed.

a. DC restorer setting

The DC restorer time constant should be selected for optimum display of the received data. Too short a time constant will cause fade-out of large areas of constant intensity (i.e., a peaking of the leading edges with gradual fall off, toward the average intensity level, as scanning progresses), while too long a time constant will not permit the system to respond to rapid changes in average intensity which may be occurring. A good method of selection is to choose the fastest time constant which does not produce fading of the largest areas of constant intensity present in the received data. For most data the medium time constant setting will be satisfactory.

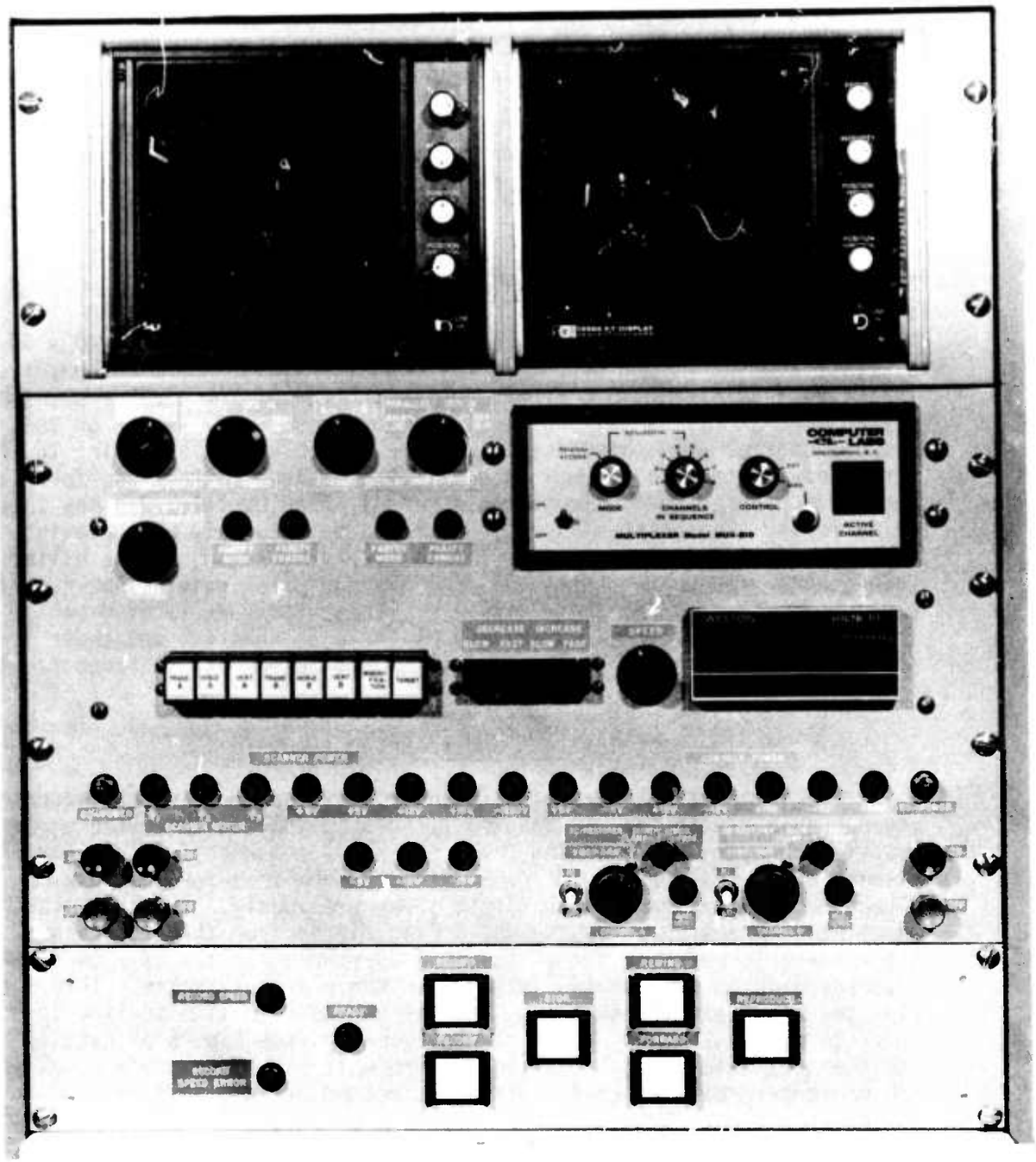



Fig. 1. Console Control Unit, system operating controls.

If a very good signal to noise ratio is available, the clamp mode of the DC restorers may be used. As discussed earlier in Chapter II, in this mode the IR detector dark level is clamped to the lower edge of the signal input range giving the maximum possible dynamic range for data display and recording. If the noise level is too high, however, alternate scanning lines (vertical lines on the display units) will vary in intensity in a random manner, making this mode unsuitable for use.

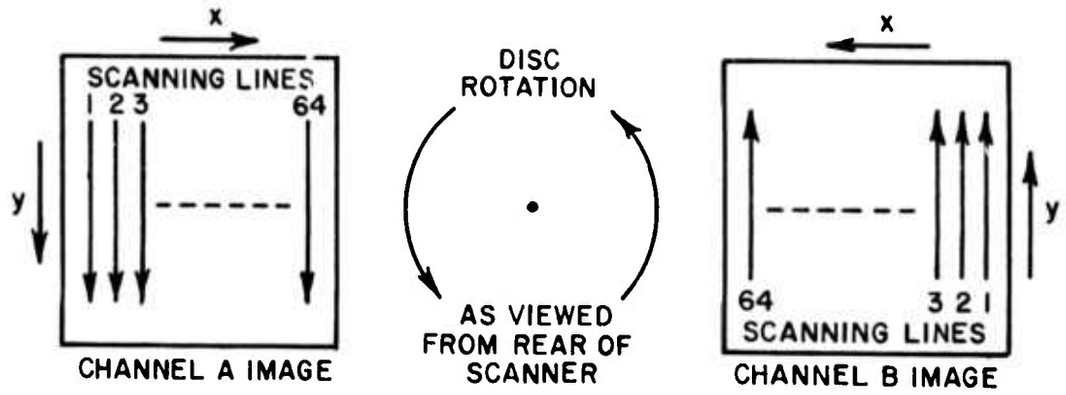
b. Playback of a pre-recorded tape of opposite format

If it is desired to play back a pre-recorded tape having 40 x 40 element, 200 frames per second format when the system has been converted to the 64 x 64 element, 60 frames per second format, or vice versa, this may be done simply by setting the Image Format selector switch on the console control unit chassis (see Note below Table III) according to the format of the tape to be reproduced. The detailed instructions for playback of a pre-recorded tape given in Ref. 1, Chapter III-B-2-d may then be followed. To obtain minimum error rate, particularly when playing back 40 x 40 format tapes, it may be necessary to re-adjust the Miller Code decoder center frequency pots for minimum error rate as shown by the error indicators and/or image displays. These pots are located behind the front panel on the tape recorder Miller code chassis, and their positions are indicated by the diagram on the inside of the front panel.

3. Image orientation and scanning sequence

The information concerning image orientation and display sequence given previously in Ref. 1, Chapter III-B-3 is applicable to the present system. However, the scanning (and recording) sequence for the 64 x 64 element 60 frames per second format differs from that for the 40 x 40 element 200 frames per second format given previously. In particular, the line scan sequence for channel B must differ from that for channel A since there is only one set of scanning apertures for the 64 x 64 format scanning disc instead of two sets, as in the previous system. This fact, plus the fact that the sampling interval varies from line to line in order to obtain lines of equal physical length (see Fig. 5 of Ref. 1) and that channels A and B data points are multiplexed to use a single A/D converter requires that a different method of interlace be used to avoid interference between A channel and B channel data. The scanning sequence for the 64 x 64 element per frame format is given in Fig. 2. The order in which information is written on tape is the same as the scanning sequence.

The display sequence is the same as given previously (Ref. 1, Fig. 14), consequently A channel images are inverted (top-to-bottom) and B channel images are reversed (left-to-right) on all display indicators as compared to image orientation at the scanner input aperture. It may be desirable, particularly if both channels are used to scan a single




EACH VERTICAL SCANNING LINE CONTAINS 64 WORDS SCANNED IN SEQUENCE (1,2,---64) AS INDICATED BY DIRECTION OF ARROW

CHANNEL A HORIZONTAL SCAN IS INTERLACED WITH LINE SEQUENCE (1,3,5,------63,2,4,6,------64)

CHANNEL B HORIZONTAL SCAN IS INTERLACED WITH LINE SEQUENCE (2,4,6,------64,1,3,5,------63)

Fig. 2. Scanning sequence for 64 x 64 element format.

64 x 128 element image, to change polarity connections to the console display indicators to obtain proper image orientation as suggested in Ref. 1, Chapter III-B-3.

## IV. THEORY OF OPERATION

This chapter contains details of the individual units, circuit groups, and logic cards comprising the 2-channel infrared scanner system which have been modified or added as a result of conversion of the system from the original 40 x 40 element, 200 frames per second format to a 64 x 64 element, 60 frames per second format. The new logic is compatible with both formats and is switch selectable (via two Image Format switches, one on the console control unit chassis and the other on the scanner relay panel) so that either may be used as desired. (Changing scanning format requires interchanging the scanner sub-assemblies - see Appendix III.)

Circuit and logic diagrams for the circuits discussed in this chapter are given in Appendix I. Those circuits and logic cards which remain unchanged are not included in this chapter (nor in Appendix I) since they have been covered previously in Ref. 1.

## A. Logic Wiring Diagrams

Logic wiring diagrams for the telescope-mounted package (scanner and scanner control unit CU-2) and for the system control package (console units and magnetic tape recorder) are given in Figs. 3 and 4, respectively, of Appendix I. Functional circuit groups and/or circuit boards are shown on these diagrams as appropriately labeled rectangles with interconnections shown and directions of signal flow indicated. Card slots occupied by all printed circuit cards are given by the circled numbers within the rectangles, and card cage pin numbers are given for all interconnections to each card. Interconnections labeled "Front Edge Connector" are made via the special edge connector bolted to the front edge of a circuit card, while all other interconnections are made via the standard card cage (rear edge) connectors. Where signal paths are completed via intervening connectors, the corresponding connector numbers are given.

In addition to providing detailed information on the various circuit groups and signal paths, these diagrams show all card cage connections, and hence serve as card cage wiring diagrams. All circuit cards for the telescope-mounted package are located in the scanner control unit CU-2, while all cards for the control package are located in the console mounted scanner logic unit SLU-1.

Certain components such as channel selectors and video gain controls included in these diagrams for functional completeness may be found in more detail in schematics for the specific units containing them (see Section B. below).

The general theory of operation for the complete system, for which these diagrams illustrate all logic components, has been presented previously in Chapter II and/or in Ref. 1, Chapter II. Additional details of individual components are given below and in Ref. 1, Chapter IV.

## B. Major System Components

### 1. Scanner

A general description and photographs of the scanner unit are given in Ref. 1, Chapter IV-B-1. A new schematic diagram is given in Fig. 5 (Appendix I) of this report which replaces Fig. 22 of Ref. 1. Changes made include new scanner motor specifications, a new 6 volt power supply to replace the former +5.5 volt supply, and addition of an Image Format selector switch (physically mounted on the lower edge of the stepping motor relay panel - item 22, Fig. 16, of Ref. 1).

### 2. Scanner control unit

A description and photograph of the scanner control unit is given in Ref. 1, Chapter IV-B-2. The previous wiring diagram, Fig. 24 of Ref. 1 is replaced by Fig. 6 of this report. The principal change is the added wiring for the Image Format switch mentioned above.

### 3. Console control unit

The console control unit is described in detail in Ref. 1, Chapter IV-B-3. A front panel photograph of this unit, as modified, is given in Fig. 1 of this report, and a new wiring diagram is given in Fig. 7 which replaces Fig. 25 of Ref. 1. Changes include addition of the front panel switches for DC restorer control and the chassis-mounted switch for Image Format selection.

### 4. DC power supplies

The +5.5 volt power supply listed in Table VII of Ref. 1, Chapter IV-B-5 has been replaced by a new (+6 volt nominal, 6 amps. max.) supply having a greater capacity and better temperature stability. This supply, which drives the sync projector lamps (PSI of the scanner, Fig. 5 of this report) should be set to approximately +5.8 volts for the original 40 x 40 element scanner sub-assembly and to approximately +6.5 volts for the new 64 x 64 element scanner sub-assembly. The voltage may be adjusted to some degree during system alignment. A higher voltage gives increased illumination and consequently greater amplitude (or steeper rise time) sync pulses, but decreased lamp life; consequently, the lowest voltage setting producing adequate illumination should be used.

Connections and specifications for this supply are included in Fig. 5. The diagram for the former +5.5 volt supply, Fig. 30 of Ref. 1, is now obsolete.

## C. Logic Circuits

### 1. Video preamps

The time constants of the coupling circuits between the Perry preamps (mounted in the scanner unit) and the video preamps (scanner control unit logic card) have been modified for optimum performance with the DC restorer system. A new schematic diagram of the video preamps including these changes is given in Fig. 8 which replaces Fig. 31 of Ref. 1. Other details concerning the video preamps are given in Ref. 1, Chapter IV-C-1.

## 2. Sync projectors and detectors

The sync projectors and detectors used with the 64 x 64 element scanner sub-assembly are essentially the same as the original units described earlier in Ref. 1, Chapter IV-C-2. The illumination system has been modified however, and the reticles are different as described earlier in Chapter II-B of this report. The new projectors use GE type 1493 6.5 volt lamps. Lamp replacement and sync system alignment are essentially the same as previously described in Ref. 1 (Appendix IV) for the 40 x 40 element scanner sub-assembly with evident changes with regard to lamp type and image format.

## 3. Video filters

The video filter logic board has been modified to include the unity gain feedback amplifiers used with the video DC restorers as discussed earlier in Chapter II-B. A new schematic diagram including these amplifiers is given in Fig. 9 which replaces Fig. 37 of Ref. 1. As shown in the diagram the video inputs (for channels A and B) are applied to the non-inverting inputs of these amplifiers while the DCR feedback signals (from the D/A converters located on the data clock board) are applied to the inverting inputs to shift the baseline as required for clamping or DC restoration. Trim pots are provided to set the outputs to zero with no input signals applied. The amplifier outputs drive the video filters which are identical to those previously described in Ref. 1, Chapter IV-C-6.

## 4. DC restorer

A general description of the digital dc restorer and its operation has been given in Chapter II-B of this report. A logic diagram is given in Fig. 10 and the interconnections with other parts of the video system are included in Fig. 4. A separate DC restorer logic card is used for each video channel.

With reference to Fig. 10, if one of the DC restorer positions, FAST, MED., or SLOW, is selected (via the selector switch on the console control unit front panel), each write strobe input is applied to the up-down counter (SN 7493-9,8,5,2, and 1) causing it to count. If the most significant bit of the A/D converter output is "1" (i.e., if the associated video data point is positive) the write strobe is gated to the up-count input causing the counter to increment, while if the most significant bit is "0" (i.e., if the associated data point is negative), the write strobe is gated to the down-count input causing the counter to decrement. Thus the counter output at any time is the difference between the number of positive data points and the number of negative data points which have occurred prior to that time. The counter output is applied, in 8-bit binary form, to a D/A converter (located on the data clock board - see paragraph 10, below) producing an analog signal proportional to the

average baseline offset which is then applied to the inverting input of a unity gain video amplifier (located on the video filter board - see paragraph 3, above), tending to move the baseline back toward zero.

The effective time constant of the circuit may be selected by controlling the effective "gain" of the counter circuit. This is done by by-passing one section of the counter (SN 74193-9, containing 4 binary stages) to obtain the med. time constant and two sections (SN 74193-9 and -8) to obtain the fast time constant via the gates, SN 7432-7 and SN 7408-6; while all sections are used to obtain the slow time constant. Thus successive steps of the time constant selector switch vary the effective circuit time constant by a factor of 16.

If the DC restorer selector switch is set to the CLAMP position, the counter is disabled via a "0" level applied to the load input of counter section SN 74193-5 loading this counter with zeros (hard wired) and inhibiting counting, thus isolating the final sections SN 74193-2 and -1. Line sync is enabled (via the gates SN 7400-3 and SN 7402-4) and applied to clear these two sections of the counter thus setting their outputs to zero and applying, via the D/A converter, a zero input to the inverting input of the unity gain video amplifier. Then when the sample strobe input occurs, somewhat later in time (see the B-sync generator timing diagram - Fig. 12) but still during the dark space between scanning lines, the video output with the IR detector dark, and with no offset bias applied to the unity gain amplifier, is measured via the A/D converter and applied to the data inputs of the final counter stages SN 74193-1 and -2. This data is latched into the counters (which now serve as data storage registers since no down-count or up-count inputs are applied) by the trailing edge of the sample strobe, and thus appear at the counter outputs throughout the scanning of the next data line. An analog voltage proportional to this output is generated by the D/A converter and applied as offset bias to the unity gain video amplifier effectively clamping the video dark level, measured during the sampling interval, to the lower edge of the video signal input range. This value of offset voltage is held until the next line sync pulse occurs at which time the cycle is repeated.

### 5. Sync separator

The sync separator remains unchanged and has previously been described in Ref. 1, Chapter IV-C-8. However, the disc sync portion of this circuit is not used (as mentioned previously in Chapter II-B) when the 64 x 64 element scanner sub-assembly is installed, and when interchanging scanner sub-assemblies slight readjustment of the line sync and frame sync delay pots may be required to achieve optimum performance (see Appendix IV-C-1 and IV-C-3 of Ref. 1).

## 6. B-sync generator and digital data demultiplexer

The B-sync generator and digital data demultiplexer logic circuits currently used are quite similar in function and design to those originally described in Ref. 1, Chapter IV-C-9. There are several significant changes, however, in various parts of the circuit so that correlating the changes with the original circuit description is difficult. Consequently, the complete description for the modified circuit is given below and is to replace the reference cited above. Functionally, the changes include switch selectable timing changes for the two image formats, generation of signal waveforms for obtaining the dark space sample points (used by the CLAMP mode of the DC restorer circuit - see paragraph 4, above), and modification of the next channel address timing to provide greater tolerance for proper operation when the disc scanning apertures vary with respect to their ideal locations. A logic diagram of the modified circuit is given in Fig. 11 and the corresponding timing diagram is given in Fig. 12. These figures replace Figs. 41 through 43 of Ref. 1.

Several additional synchronization signals which can be derived from the Channel A raster word sync and A line sync signals are required throughout the system. These signals, B raster word sync, B line sync, A data register line sync, B data register line sync, channel address, and channel transfer, are obtained via the B-sync generator. Closely related signals, A data strobe and B data strobe, are also required for demultiplexing the digital data following analog multiplexing and A/D conversion; and similar signals, A sample strobe and B sample strobe which occur during the dark space between data lines are used in conjunction with the video DC restorer clamp mode. These are generated from the present channel address and data ready signals from the multiplexer and A/D converter, respectively, by the digital data demultiplexer mounted on the same circuit board. Additional information concerning the requirements and derivation of the various word sync related waveforms generated by these circuits is given in Appendix II of Ref. 1.

The Channel B line sync and raster word sync signals are obtained from the corresponding Channel A signals via a delay equal to ½ the word spacing of the shortest raster line. This delay is provided by the B-channel delay 1-shot (see Figs. 11 and 12) which is triggered by each A line sync or A raster word sync input pulse. Note that two B-channel delay 1-shots are provided, one (pre-timed) for each image format. The appropriate one is selected via the Format input (from the console control unit Image Format switch) while the other is disabled via a zero level applied to the clear input. Output pulses of apprxoimately 120 ns duration are generated following each delay gate by the B-delay pulse generator 1-shot. The A line sync input pulse also sets the A data register line sync flip-flop (composed of two sections of the SN 74279-6 R-S flip-flop connected to produce both "Q" and "$\overline{Q}$" outputs) while the first A raster word sync pulse clears this flip-flop generating the required output waveform having a negative-going transition coincident with the first word sync pulse of each data line. The

outputs of this flip-flop are also used in conjunction with two AND gates (SN 7408-9) to demultiplex the B line sync pulses and B raster word sync pulses onto separate output lines.

The B line sync and B raster word sync waveforms are then used to generate the B data register line sync output via an additional flip-flop as was done for A channel, above.

The channel A and channel B raster word sync pulses (used by the raster generators for analog video display) occur at the beginning of each data word interval (i.e., just as the disc begins to scan the corresponding image element). Sampling for A/D conversion however should occur at the center of each image element and, since a single A/D converter is used for both channels, samples from the two image channels must be multiplexed. Generation of the required waveforms, channel transfer to initiate sampling, and channel address to designate the channel to be sampled, will now be described.

The A raster word sync and B raster word sync pulse trains are individually delayed (by ½ the word spacing of the shortest data line minus the multiplexer set-up time) by means of the A channel transfer delay 1-shot and B channel transfer delay 1-shot, respectively, and their associated pulse generator 1-shots. (Two delay 1-shots are actually provided for each position with selection via the Format input, as above.) Line sync pulses are also applied to the channel transfer dealy 1-shot inputs to produce the necessary pulses for the dark space sample points. The delay pulse generator outputs are then ORed together via the NAND gate (SN 7400-7) and applied to trigger the channel transfer pulse generator 1-shot (to provide a delay relative to the next channel address waveform) thus producing the required channel transfer signal output. Outputs from the B-delay pulse generator and A-delay pulse generator are applied to set and reset, respectively, the next channel address flip-flop which thus provides the correct channel address to the multiplexer prior to initiation of sampling via the channel transfer pulses.

Digitized samples for both A and B channel video appear, multiplexed, on the 8 A/D converter output data lines (see Fig. 4). These are demultiplexed by strobing the data from the lines into the appropriate registers or other circuits via the A data strobe or B data strobe, as required. These strobes are generated by the digital data demultiplexer which consists of the two upper AND gates (SN 7408-9), and four lower AND gates (SN 7408-10), and associated inverters, of Fig. 11. The data strobes (and dark space sample strobes) originate as the data ready pulse generated by the A/D converter each time a new sample is available on the data output lines. This pulse is routed to either the A-channel or B-channel output lines via the two upper AND gates driven by the present channel address waveform from the multiplexer. Data strobes and dark space sample strobes, which appear on the same lines up to this point are demultiplexed by the four lower AND gates driven by the A and B data register line sync waveforms.

The timing waveforms given in Fig. 12 are for the longest raster line, 40 x 40 format, at 200 frames per second, and represent essentially the "worst case" conditions in that time intervals (for sync pulses, dark space sample points, etc.) within the dark space between data lines are minimum. The values in parentheses are for the shortest raster line, i.e., line 40 to line 1 of the 40 x 40 format, while time intervals for the 64 x 64 element, 60 frames per second format will be greater than those indicated. The waveforms of Fig. 12 are drawn approximately to scale with the width of short pulses exaggerated to show leading and trailing edges more clearly.

### 7. Multiplexer and A/D converter

The multiplexer and A/D converter have been described previously in Ref. 1, Chapter IV-C-11 and 12. Supplementary timing diagrams for these units as used in the present system are given in Figs. 13 and 14 of this report.

### 8. Digital video driver

Because of the added loading produced by the modified data register system (see below) and the DC restorer circuits the internal A/D signal output drivers are inadequate, particularly in their capability for current sinking in the "0" state. Consequently, a digital video driver circuit board has been added. This circuit, shown in Fig. 15, consists of 8 NOR drivers (SN 7428), one for each data line, operated as inverting buffer amplifiers driven via inverters (SN 7404) to preserve the previous signal polarity.

### 9. Parallel input - serial output encoder

The parallel input-serial output encoder has been described previously in Ref. 1, Chapter IV-C-13. However, system modifications to accommodate the 64 x 64 element image format required considerably more temporary data storage than that previously used, consequently a simple modification of the previous encoder (data register) was not feasible and a new system employing different storage techniques has been implemented. Although the general function of the encoder remains essentially the same as before, the logic circuitry is considerably different as described below. In addition to the increased storage, the new encoder system uses two logic boards common to both A and B channels while for the former system each channel was completely independent. The new approach not only eliminates duplication (which as a secondary benefit made two additional card slots available for the DC restorer circuits) but also permits simplification of timing requirements for computer loading of data during playback by ensuring that corresponding data points for A and B channels are recorded simultaneously.

The new parallel input-serial output data encoder (Data Register of Fig. 4) will now be described with reference to Figs. 16 and 17. This section, and the associated figures, replace Section IV-C-13 and Figs. 46 and 47 of Ref. 1 which are now obsolete.

Digital video data available from the A/D converter is in parallel, 8-bit binary form. In addition, because of the scanning method used (see Ref. 1, Chapter II), the data is asynchronous. As discussed previously parallel recording on separate tracks at the required data rate is not feasible because of dynamic skew limitations, hence a high density serial recording (Miller Code) technique utilizing a single magnetic tape track for each video channel is used. The required format which combines video, sync signals, and an optional parity check in a single, synchronous, serial data stream for application to the Miller Code system has been given previously in Fig. 7, Ref. 1. The purpose of the parallel input-serial output encoder is to generate this serial data stream from the available input data and sync signals.

Data register boards 1 and 2 are common to both channels. Board 1 contains a parity generator, and logic circuits for mode selection, format selection, sync code generation, and various control waveforms required by the data registers, while Board 2 contains data strobe delays, read and write address counters, and a comparitor for controlling register output. A separate data register Board 3 is used for each channel. Each of these boards contains eight 4 x 4 register files connected to provide sixteen 8-bit words of temporary storage, data selectors for address selection and output data or sync code selection, and an 8-bit parallel-input serial-output shift register for parallel to serial conversion.

The basic function of the encoder is to convert the asynchronous parallel input data, plus synchronization signals required for raster generation at playback, to a synchronous serial bit stream suitable for the Miller Code system. This is accomplished by means of the shift register which may be loaded with data from the register files, a 4-bit sync code, or 0101 preamble or gap filler code as determined by the control logic. The remaining logic circuits of the encoder control the addressing, loading and unloading of the register files, parity generation, mode and format switching, and appropriate start and stop sequences for the decoder when the recorder is switched on and off, respectively.

Since data input is asynchronous (i.e., data for each image line comes in a burst at an input frequency peculiar to that particular line (but exceeding the output data rate), followed by a gap of varying length prior to arrival of data for the next line) while data output is synchronous, temporary data storage must be provided within the encoder. This is provided by the register files. These are loaded in sequence as input data arrives; and are unloaded, in sequence, at a constant rate determined by the output data clock. For the input and output data rates used for this system, 16 data registers are sufficient to insure that at least one empty data register is available whenever input data arrives, even allowing for possible variations in scanning speed (determined by the instantaneous speed of the synchronous scanning disc motor).

For a continuous system such as this, average input and output data rates must obviously be identical. Also, the output bit rate must be a known constant in order for the Miller code system to function properly. These requirements are met while still permitting small variations in scanning speed via the variable length 0101 gap filler code (see Fig. 7, Ref. 1). Since the 101 sequence is used by the Miller code system at playback to recover the data clock from the recorded data, this gap filler code, together with the preamble and any 101's occurring in the video data, also helps insure proper clock synchronization during playback.

Operation of the data encoder will now be described with reference to Figs. 16 and 17.

Data input lines for the seven most significant data bits are hard wired to the parity generator (Board 1) and to the data inputs of all register files (Board 3), while the least significant bit data input for each register file is supplied (from Board 1) by either the parity bit or the least significant data bit as determined by the mode selected. Channel A and Channel B video data are multiplexed on these data lines as discussed previously. The appropriate register is parallel loaded with this data by strobing the write enable input of that register when the desired (Channel A or Channel B) data is present on the input lines. The required data strobe enters the encoder (Board 2) from the digital data demultiplexer (paragraph 6), is delayed by 40 ns (i.e., the width of the input pulse) and lengthened to 100 ns by the data strobe delay 1-shot, and is then routed to the appropriate register write enable input via the write strobe selector (Board 3) under control of the input address counter (Board 2). The delay is required to insure sufficient time for generating the parity bit and to permit reset of the input address prior to loading.

The 0101 preamble and gap filler code is generated by the clock divider (Board 2) from the data clock waveform and is automatically loaded into the output shift register (Board 3) via the serial input whenever the register is clocked for output. This code may either be retained for output or be replaced by data or sync code via the parallel inputs, as appropriate.

Sync code is generated by the sync code register (Board 1) and may be parallel loaded as required into the four highest order bit positions of the output shift register via the sync code selector (Board 3). Line sync code (0000) is generated by clearing the sync code register (via the inverted B line sync pulse) while frame sync code is generated (for the first data word of each frame) by subsequently clocking the sync code register (via the inverted frame sync pulse) to produce the required code, 0011 (for the 8 data bit mode) or 1100 (for the parity check mode), as determined by the register D inputs driven by the mode flip-flop (Board 1).

Assume that the system is in steady state operation and is, at the moment, clocking out gap filler code after completing the data output for the previous line (a process which will be described later). The loading sequence for the new data line is then as follows (see Fig. 17, Sheet 1):

A B line sync pulse is first received indicating that data words for the new line will be available within several microseconds (see Fig. 17, sheet 1). This pulse is applied to the clear inputs of the sync code register thus loading the line sync code. If the new line also happens to be the beginning of a new frame, a frame sync pulse is received approximately 3 μs after the line sync pulse. This pulse is then applied to the sync code register clock inputs thus changing the line sync code previously loaded to frame sync code.

Next, the first A data strobe is applied (via the upper NAND gate SN 7420-7 controlled by the strobe selector flip-flop, Board 1) to reset the input address counter (Board 2). The delayed data strobes (A and B write strobes from Board 2) then load the first data word for each channel into the first register file (address 0000). The trailing edge of the B write strobe then increments the input address counter prior to receipt of the next data word and disables the write address reset input (via the strobe selector flip-flop and associated NAND gate) preventing reset of the input address until the beginning of the next data line.

Subsequent write strobes then load the remaining data words of the line into the register files in sequence. Since only the first four stages of the input address counter are used to determine the input address via the write select outputs, Board 2, (the last four stages are used with the word count comparitor - see below). The address automatically recycles back to 0000 after the last data register (address 1111) has been loaded and the cycle is repeated for data words 17 through 32, etc., until all data words of the line have been loaded. Input and output rates are such that data word 1 will have been unloaded from the first data register before that register is again required (for data word 17), etc., so that no over-lapping of data occurs. The loading cycle is now complete, and with the arrival of the next line sync pulse to the encoder, the cycle is repeated.

The data encoder output sequence will now be described. Data is parallel loaded into the output shift register from each successive register file (Board 3) by reading the file contents onto the output data lines (via the read select and read enable inputs under control of the output address counter) and strobing them into the shift register via a positive clock transition while shift/load is low. Then, with shift/load high, the data ia clocked out serially, a new data bit appearing at the serial data output for each positive transition of the data clock. As data bits are clocked out 0101 gap filler code is clocked into the shift register and is hence always available if needed following output of a data word. Normally a new data word is loaded immmediately after output of the previous word, however, after the last word of a

line has been clocked out the gap filler code is clocked out until data for the next line becomes available.

Inputs from two crystal controlled clock oscillators (from the data register clock board - see paragraph 10 below) are available. One for each of the two image formats. The appropriate one is selected via the format selector (Board 1) and is divided by two via the clock divider to provide the data clock waveform, 2.716 MHz for the 40 x 40 format, or 2.29 MHz for the 64 x 64 format. This data clock signal drives the output shift register (Board 3) and is also applied, together with the serial data output, to the input of the Miller code magnetic tape recording system.

Control of the output shift register (Board 3) to assemble and output the required serial data stream is accomplished by means of the shift/load and sync select waveforms generated by the control logic of Board 1. This control logic includes the strobe selector flip-flop, and the associated NAND and NOR gates (Board 1). The data enable output from the word count comparitor (Board 2), which determines whether more data words per line yet remain in the register files is also utilized. The inter-relationships between these various components and associated waveforms are given by the timing diagram, Fig. 17, Sheet 2).

Now assume the system to be in steady state operation with 0101 gap filler code being clocked out as before. Further assume that B line sync, and frame sync, if present, have been received thus loading the sync code register and clearing the strobe selector flip-flop (Board 1). Now when the trailing edge of the first B write strobe occurs (see Fig. 17, sheet 2), indicating that the first data word of the next line has been loaded and is available for output, the strobe selector flip-flop is set which, in turn, sets the data-ready flip-flop and enables the output reset flip-flop via its D input. Upon completing the output of the current 01 bit sequence of the gap filler code which may be in progress when the output reset flip-flop is enabled, the leading edge of the B output from the clock divider is applied to set the output reset flip-flop. The output of this flip-flop is gated with the clock divider B output (for proper timing) to generate the sync select pulse which, via the sync code selector (Board 3) applies the contents of the sync code register to the four highest order (first out) parallel inputs of the output shift register. A shift/load pulse is also applied to the shift register at this time so that on the next positive transition of the data clock the sync code is loaded and appears at the output, in serial form, during the next four data clock cycles.

The trailing edge of the sync select pulse triggers the output reset 1-shot which resets the output address counter ( thus addressing the first data word of the line for output), the clock divider (to initialize the bit counting sequence for the new series of data words), and the data ready and output reset flip-flops (preparing them for a subsequent data line).

Assuming that the data enable flip-flop is set (i.e., a start-up time delay sequence is not in progress - see below), outputs B, C, and D of the clock divider (which functions as a data word bit counter) are combined with the data enable (address comparitor) signal and the sync select signal to generate the shift/load waveform for the data line. This signal causes the first data word to be loaded into the output shift register immediately following output of the sync code, and subsequent words to be loaded contiguously until all data words of the line have been output. The output address counter is incremented following each shift/load pulse (except for the initial one of each line used to load the sync code) so that the correct address for each subsequent data word is obtained.

Following loading of the last data word of the line into the output shift register the input count is no longer greater than the output count and the shift/load waveform is gated off via the data enable output from the address comparitor. (Actually, the data enable signal switches on and off alternately near the beginning of a data line as data words are loaded and unloaded, but is on when needed to gate the shift/load waveform. Later, as a surplus of data words accumulates in the register files it remains on until finally it turns off again after all words of the line have been unloaded.) Hence, further parallel loading of the output shift register is inhibited and, following output of the last data word, gap filler code (automatically loaded at all times via the shift register serial input, as mentioned previously) is output until sync code for the next data line has been loaded initiating a new output data cycle, as above. Note that the 0101 preamble (see Fig. 7 of Ref. 1) is obtained as the last 4-bits of the gap filler code in the present system, rather than being loaded simultaneously with the sync code as was done previously.

The above descriptions of the input and output sequences assume steady state operation. If the first data frame recorded after turn-on is to be recoverable during playback, three additional requirements must be met: (1) some means must be provided for synchronizing the Miller code output data clock at playback prior to arrival at the first actual data, (2) data recording must start at the beginning of a data frame, and (3) input and output address counters must be reset prior to inputting the first data frame to the encoder.

The requirement for clock synchronization at playback is met by recording a series of 0101 sync code for a period of approximately 5 seconds following recorder turn-on prior to recording of the first data frame. The start of actual data recording is triggered by arrival of a frame sync pulse, hence data recording always begins at the start of a new frame; and finally, proper reset of the input and output address counters is accomplished at the beginning of the first frame in the same manner as for steady state operation. Operation during recorder turn-on will now be described with reference to Fig. 16 and Fig. 17, sheet 3.

Prior to recorder turn-on the encoder operates as in steady state with input and output exactly as previously described. The output is, of course, not being recorded, but it may be viewed on the visual display indicator if desired by setting the selector to the SERIAL IN position. If the two RECORD buttons on the recorder front panel or recorder control unit are now pressed, the tape will accelerate to recording speed and the pinch rollers and recording heads will then close. At this time the record relay in the recorder control unit (Fig. 28 of Ref. 1) will close (see Fig. 17, sheet 3). Contacts of this relay are indicated by the Recorder off-on switch of Fig. 16, and as shown in this figure, the on position applies a 0 level to the on-off flip-flop D input so that this flip-flop is reset when the next frame sync pulse arrives. The output of this flip-flop triggers the 5 second start-up delay 1-shot. During the timing cycle a 0 level is applied to the D input of the data enable flip-flop by the 1-shot. When the trailing edge of the frame sync pulse occurs the data enable flip-flop is reset. The output of this flip-flop is applied to disable the read counter drive and the shift/load input to the output shift register thus insuring that 0101 gap filler code (loaded via the serial input) is output during the timing interval. Since line sync and frame sync are not inhibited during the start-up delay the sync register loading cycle will have occurred (many times) during the timing interval and hence the required sync code will be available for the first recorded data frame. The input data loading cycle is also continued during the timing interval, but the data is not used (since shift/load is disabled) and both input and output counters are properly reset for the first recorded data frame as for steady state operation described above.

At the end of the start up delay a 1 level is again applied to the D input of the data enable flip-flop and when the leading edge of the next frame sync pulse occurs, this flip-flop is set returning the system to normal operation.

When the RECORD mode is turned off (either by the operator, or when end-of-tape is reached) a true level is applied to the D input of the on-off flip-flop which then sets when the next frame sync pulse arrives thus completing the on-off cycle at the end of the current data frame. No other change in encoder operation occurs at this time and the encoder output, though no longer being recorded. can still be viewed on the visual display indicator as desired.

A mode selector switch which may be used to select 8 data bits per word, or 7 data bits plus parity, for recording is located on the front panel of the console control unit. This switch. shown schematically in Fig. 16, sets the D input of the mode flip-flop to 1 or 0 for the 7 bit plus parity mode or the 8 data bit mode, respectively. Coincident with the leading edge of each frame sync pulse, the D input of the flip-flop is clocked to the output and remains until a subsequent change in D input followed by a frame sync (clock) pulse occurs. Thus the position of the mode switch may be changed at random, but actual switching of the encoder logic will only occur prior to the beginning of a new frame so that no

errors are introduced by changing the position of the mode switch while recording is in progress. Timing diagrams for mode switching are given in Fig. 17, sheet 3. Note that loading of the frame sync code (which is determined by the mode selected) is delayed until the trailing edge of the frame sync pulse occurs (see Fig. 17, sheet 1) so that the proper code will be loaded for the frame immediately following a change in mode, as well as for all subsequent frames.

The outputs of the mode flip-flop are applied to the D inputs of the sync code register to provide the proper frame sync code for each mode, and to the gating inputs of the mode selector (Board 1) used to select either the least significant data bit or the parity bit for the eighth bit applied to the register file inputs. The parity bit is generated from the seven higher order data bits by means of a parallel input parity generator (Board 1) wired to generate even parity. Note, however, that the AND-NOR used to select this bit produces a data inversion so that odd parity is actually output by the encoder when the 7 bit plus parity mode is selected and, when the 8 data bit mode is selected, the least significant data bit is inverted. The data is recorded in this manner, but the inverted bit is reinverted by the decoder during playback.

### 10. Data register clock and DCR D/A converters

The data register clock and output buffer PC board previously described in Ref. 1, Chapter IV-C-14 is obsolete and has been replaced by the data register clock and DCR D/A converter PC board described in this section. The schematic diagram for this board is given in Fig. 18 which replaces Fig. 48 of Ref. 1.

The new board contains only the two crystal controlled clock oscillators, one for each of the available image formats (5.432 MHz for the 40 x 40 format, and 4.58 MHz for the 64 x 64 format), and two digital to analog converters (one for each video channel) used in the digital dc restorer circuits (see paragraph 4 above).

Both clock oscillators run continuously whenever the system power is on. The desired clock frequency for the image format in use is selected within the serial input-parallel output encoder, Board 1, as previously described (paragraph 9, above). The clock divider is also incorporated in the encoder and hence is not required on the data clock board.

The line length counter and output data buffer formerly included on the data clock board have been eliminated by redesign of the encoder. The line length counter has been replaced by the word count comparitor (see paragraph 9, above) so that encoder operation is independent of line length, and the output shift register serves also as an output buffer since use of a common clock to control all shift register functions eliminates any jitter in the data output as was present with the previous encoder.

## 11. Serial data decoder

The serial data decoder has been described previously in Ref. 1, Chapter IV-C-16. The decoder circuit, and consequently the description and associated diagrams (with one exception - see below) remain essentially unchanged for the present system.

However, as described in Ref. 1 (p. 65) the end of each data line must be detected via a word counter and NAND gate and hence, to provide switch-selectable compatibility with both image formats provisions had to be made to electrically select the corresponding line length. This has been done by including a word count selector controlled by the format input (see Fig. 4) in a new data decoder Board 1 for the present system. The logic diagram for this board is given in Fig. 19 which replaces Fig. 50, sheet 1, of Ref. 1.

The two electrically selectable line lengths may be changed, if desired, by means of the word count jumpers (see Fig. 19) on the PC board which are presently set for line lengths of 40 and 64 words for the two formats now available. A few minor circuit changes have been made to gain space for the added circuitry (such as substitution of a dual 1-shot to replace two single units, and elimination of a few unused I/O connections) however, except as noted above, the new board is functionally the same as before so that the description and timing diagrams given previously (Ref. 1) remain valid.

## 12. Video display switching unit

The new 64 x 64 element image format requires that while the odd numbered raster lines are scanned for Channel A, the even numbered lines are scanned for Channel B, and vice-versa, as discussed previously in Section II-B of this report. Since the display switching is such that either display indicator may be used to view data from either channel, and since the original 40 x 40 element image format (which is retained in the present logic system for future use) does not require interchange of the even and odd line scanning sequence for the two channels, provisions for interchanging the line scan sequence when an indicator is used to display a B channel image, 64 x 64 element format, are required.

This is accomplished (automatically) by a logic gating circuit added to the video display switching unit PC board as shown in Fig. 20 which replaces Fig. 53 of Ref. 1. This circuit, consisting of the lower four NAND gates and NOR gate of Fig. 20, applies the inverted least significant bit ($\overline{1}$) of the horizontal raster output from the raster generator to the video switching and D/A converter input (see Fig. 4) when B channel, 64 x 64 element format is selected rather than the normal (1) output which is otherwise used, thus inverting the even-odd line scan sequence as required.

The remainder of the video display switching system is the same as previously described in Ref. 1, Chapter IV-C-18.

13. Raster generator

A logic diagram for the new raster generator PC board is given in Fig. 21, which replaces Fig. 54 of Ref. 1. Changes made to the raster generator include the addition of high and low speed unblanking gates and associated control logic to give a more uniform display intensity for high and low speed tape playback, and the addition of various logic gates to permit switch-selectable changes in the raster size and generation of the different horizontal interlace sequence required by the new 64 x 64 element scanning format (see paragraph II-B, above).

The vertical raster generator remains essentially as previously described in Ref. 1, Chapter IV-C-19 with the following exceptions:

The single unblanking gate 1-shot of the previous circuit (Fig. 54 of Ref. 1) has been replaced by the dual 1-shot (SN 74123-10) of Fig. 21, one section timed to provide a suitable unblanking gate width for high speed playback, and the other for low speed playback. The appropriate one is selected, and the other disabled, automatically during playback by the control logic consisting of the high speed timing gate, high speed flip-flop, and associated gates of Fig. 21. Basically, the playback speed (either high or low) is determined by comparing the time interval between the line sync pulse and the first raster word sync pulse of each data line to the fixed time delay provided by the high speed timing gate. If this time interval is less than that of the high speed timing gate, the high speed unblanking gate 1-shot is selected, otherwise the low speed unblanking gate 1-shot is used.

A timing diagram for the unblanking gate control logic is given in Fig. 22, sheet 1. With reference to this diagram, and to Fig. 21, operation of the vertical raster generator is now described. The line sync input first arrives and is applied to reset the vertical raster counters and the high speed flip-flop (which is actually the first counter stage, used separately) and to trigger the high speed timing gate 1-shot. Now if one or more raster word sync pulses are received during the timing interval (which will happen during high speed playback, but not during low speed playback), one or more output pulses are produced by the timing comparitor NAND gate. The first pulse is applied, via an OR gate, to set the high speed flip-flop thus selecting the high speed unblanking gate 1-shot while gating off the low speed unblanking gate 1-shot via its B input. (The $\overline{Q}$ output of the high speed timing gate is also applied to the reset input of this 1-shot to prevent extraneous triggering when the high speed flip-flop is reset.) The output of the high speed flip-flop, when set, is also applied to disable its own input via the OR gate so that any further input pulses which may be present do not reset the flip-flop (actually a counter) prematurely. If no pulses are produced by the comparitor NAND (i.e., the high speed timing gate ends prior to arrival of a

raster word sync pulse), the high speed flip-flop remains reset selecting the low speed unblanking gate 1-shot and gating off the high speed 1-shot via its clear input. Note that the unblanking gate 1-shots are triggered by the trailing edge of each raster word sync pulse while the selection logic operates from the leading edge of the first pulse. Hence, the selected 1-shot is able to respond to the first raster word sync pulse even though this pulse is also used for unblanking gate selection.

The outputs of the unblanking gate 1-shots (only one of which operates at any given time) are ORed and inverted via a NOR gate and serve as the blanking output used to blank the display indicators between data points. Each output is also applied to the raster step delay 1-shot to drive the remainder of the vertical raster generator as previously described (Ref. 1, Chapter IV-C-19).

The end-of-line gate and associated word count jumpers (Fig. 54 of Ref. 1) have been removed from the new vertical raster generator to eliminate the need for switching to vary the line length for the two available formats. Consequently, the vertical raster counters are now reset via the line sync pulse and operation is independent of line length up to the capacity (128 words per line) of the counters. The decrease in display unit settling time required because of this later reset time is within the range of the present display units used, and is no more severe than that unavoidably required by the new horizontal interlace format (see below).

The horizontal raster generator is functionally the same as that previously described (Ref. 1, Chapter IV-C-19) when used for the original 40 x 40 element per frame format, and, with respect to circuit logic, is identical except for the additional gating required for switching to the new horizontal format. Thus, the circuit descriptions and timing diagrams given previously (Ref. 1) still apply for operation with the 40 x 40 element format. Changes required for operation with the new 64 x 64 element format are a change in the number of image lines per frame (requiring input changes to the line count NAND) and a change in the method of horizontal interlace used (see Chapter III-B-3 and Fig. 2 of this report).

Switching of the line count NAND inputs is accomplished via the two lower NAND gates, SN 7400-6, of Fig. 21 controlled by the format input in connection with the line count jumpers which are currently wired to produce the original 40 line (up-down count) sequence (requiring an output at the count of 38, see Ref. 1) for the 40 x 40 element format and a 64 line (up count) sequence (requiring an output at the count of 62 - see below) for the 64 x 64 element format.

Operation of the horizontal raster generator for the 64 x 64 element format is given with reference to the logic diagram, Fig. 21, and the timing diagram, Fig. 22, Sheet 2, of this report.

For the 64 x 64 element format, the down-count input to the horizontal raster counter is gated off and the up-count NAND, providing the

up-count input to the counter, is gated on (via two OR gates controlled by the format input) so that the horizontal raster counter (stages "2" through "32") now operates strictly as an up-counter, cycling from 0 through 62 (by two's), and repeating, in response to the line sync input. At the count of 62 the line count NAND enables the clock input to the "1" counter so that when the leading edge of the next line sync pulse occurs, the "1" counter is set thus providing the one-line offset required for horizontal interlace. The trailing edge of this pulse recycles the main counter (stages "2" through "32") back to zero so that the count continues, 1 through 63 (by two's), completing the horizontal raster. When frame sync occurs the "1" counter is reset (plus any other counter stages which may be out-of-sequence for any reason) and the cycle is repeated for the next frame.

Note that no reset pulse is applied at mid-frame (after the count 0 through 62) so that reset of the main counter is accomplished through natural recycling of the counter at this point. Consequently, it is not possible to obtain a smaller number of lines per frame (for future system changes) by changing the line count jumpers when this method of interlace is used. (There simply was no room on the circuit board, and no available card slots for additional boards to provide the necessary logic gates to achieve this versatility.). The former method of interlace (40 x 40 format) could be changed however to provide more, or fewer, lines per frame as might be desired at some future time.

An extra, "$\overline{1}$", horizontal raster output has been provided on the new raster generator board so that the even-odd interlace sequence can be interchanged as required for the B-channel display indicators as discussed previously in Sections III-B-3 and IV-C-12 of this report.

### 14. Video level and error indicators

The video level and error indicators circuit board has been modified to provide a Max. Level Signal for the front panel indicator of the corresponding video channel (see Fig. 1) whenever a data word has the value zero, in addition to the output provided for a full scale value as discussed previously in Ref. 1, Chapter IV-C-21. This is desirable since, for the bi-polar signals and coding method used, a zero output from the A/D converter indicates a maximum analog signal input level (but of negative polarity) as does a full scale output (all 1's).

The new video level and error indicators logic diagram is given in Fig. 23, which replaces Fig. 57 of Ref. 1. Operation is the same as previously described (Ref. 1, Chapter IV-C-21) except that an all zero parallel data input will produce high level outputs from the two 4-input NOR gates (SN 7425 of Fig. 23) which are NANDed and applied to an additional NAND gate (operated as a negative OR gate) in parallel with the output of the full scale detector NAND (SN 7430). Operation from this point is as described previously in Ref. 1.

## V. SUMMARY

The dual channel, 200 frames per second, 10.6 micron infrared scanning, recording, and visual display system originally designed and built for use in atmospheric imaging and image restoration experiments has been modified for higher resolution imaging of extended targets. Either the new image format providing the simultaneous images at 64 x 64 elements per frame, 60 frames per second (which may be combined to obtain a single 64 x 128 element image), or the previous format providing two simultaneous images (with variable spatial separation) at 40 x 40 elements per frame, 200 frames per second may be used by interchanging the two scanner sub-assemblies provided. All electronic systems are compatible with both image formats and are switch selectable. Very little realignment should be required when changing image formats as most alignment-sensitive components (except for the infrared detectors which are too expensive to duplicate) are pre-aligned and permanently mounted on the scanner sub-assemblies, while timing circuits which require changing are duplicated, pre-adjusted, and electronically switched as required.

Images from each channel are recorded on separate tracks of a special (Miller code) high speed digital magnetic tape recording system in real time (at 120 ips tape speed) and may then be played back at recording speed (for viewing) or at reduced speed (for viewing and/or computer input) as desired. A separate playback, viewing, and computer interface for computer processing of the recorded data has also been designed and constructed to permit data processing and image restoration studies at a site remote from the recording station.

The scanning, recording, and visual display system is fully documented in this report, together with the previous report, Ref. 1. Documentation (in preliminary form) for the playback, display, and computer interface system has also been prepared. Both systems, together with documentation are now to be delivered to RADC for use in infrared atmospheric imaging and image restoration experiments.

# APPENDIX I
# SCHEMATIC AND TIMING DIAGRAMS

All schematic, logic, and timing diagrams for the system which have been changed as a result of the modifications discussed in this report are collected in this appendix for easy reference. Details of circuit operation are given in Chapter IV which should be consulted for additional information. Circuit descriptions and diagrams for parts of the system which have not been modified were given in Chapter IV and Appendix I, respectively, of Ref. 1.

All circuit card I/O connections (indicated by the circled pin numbers) are via the card cage edge connector unless otherwise labeled. Connections labeled "front edge connector" are via the special bolt-on connector on the opposite end of certain circuit cards.

Nearly all circuit logic elements are standard TTL integrated circuits. Details for the individual IC's may be found in the manufacturers literature[3-7].

Timing diagrams are meant to illustrate circuit operation rather than to be accurate replicas of the associated waveforms. Consequently they are idealized in the sense that propagation delays, rise time, overshoot, etc., are not generally shown. In particular, the widths of narrow pulses are generally exaggerated to show the separate effects of leading and trailing edges of the waveforms which are often of importance to circuit operation.

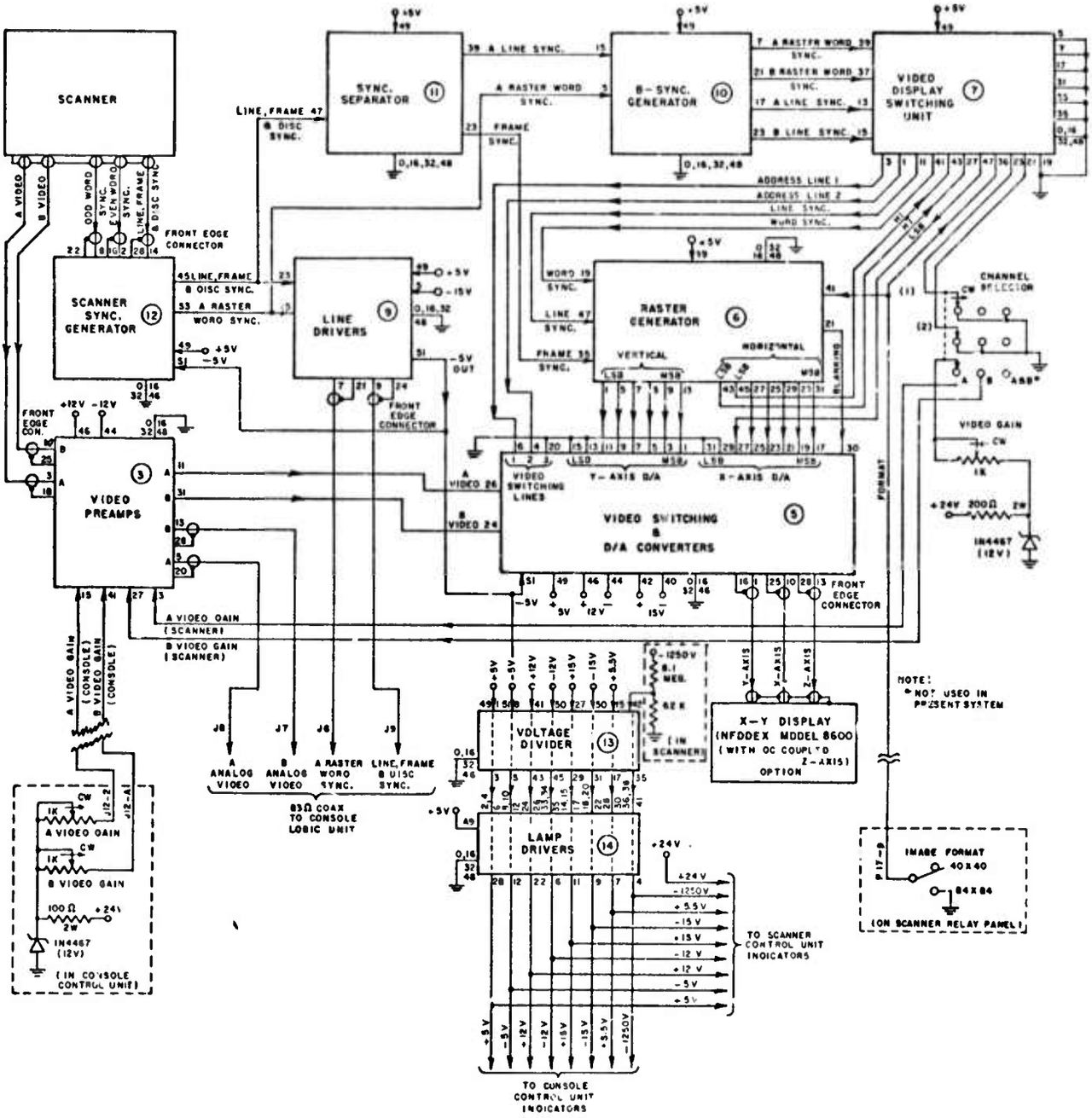



Fig. 3. Logic wiring diagram for telescope mounted package.

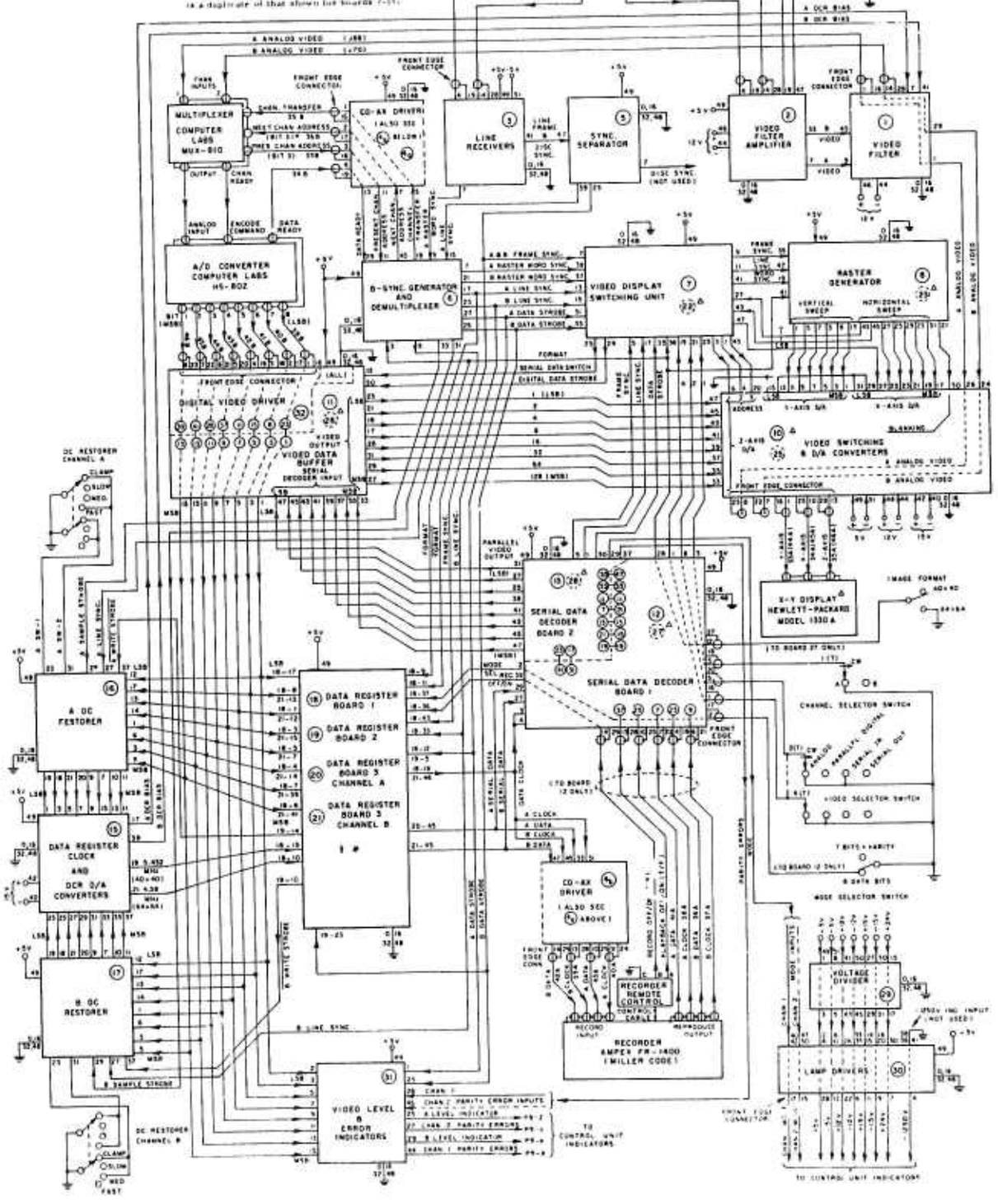



Fig. 4. Logic wiring diagram for system control package.
Sheet 1 - Console Logic

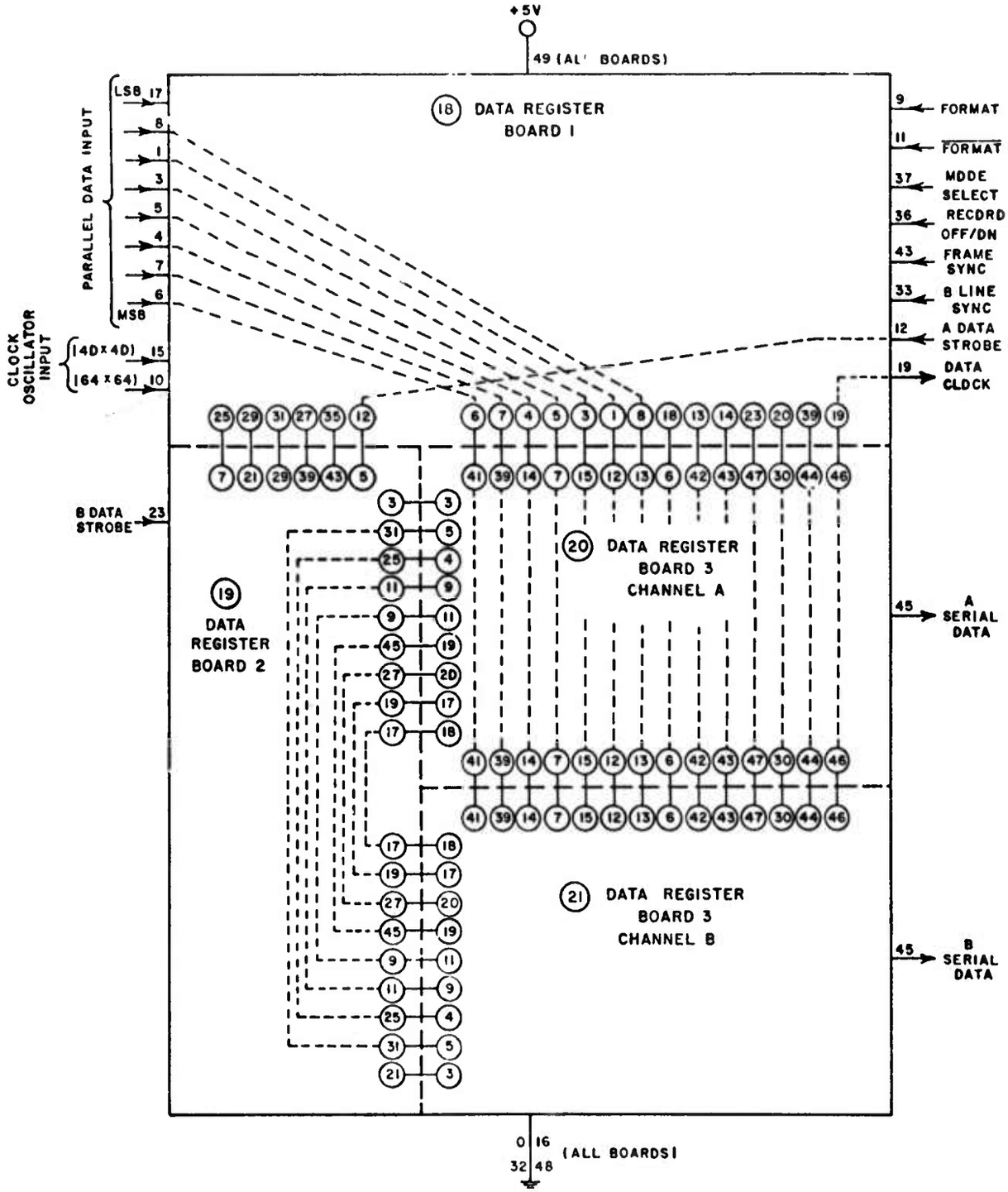
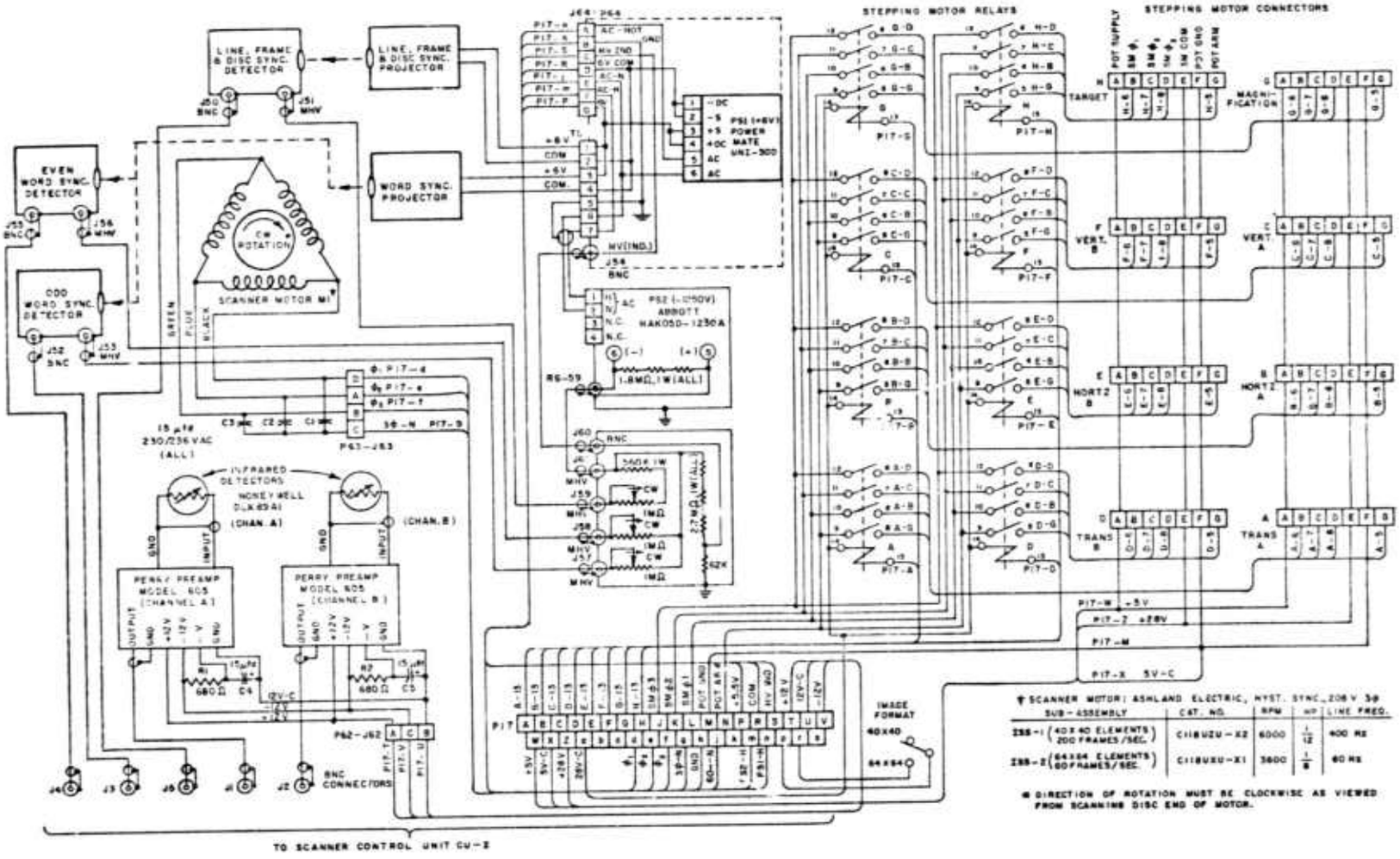



Fig. 4. Logic wiring diagram for system control package.
Sheet 2 - Data Register Interconnections.




† SCANNER MOTOR: ASHLAND ELECTRIC, HYST. SYNC., 208 V 3φ

| SUB-ASSEMBLY | CAT. NO. | RPM | HP | LINE FREQ. |
|---|---|---|---|---|
| 2SS-1 (40 X 40 ELEMENTS / 200 FRAMES/SEC.) | CIIBUZU-X2 | 6000 | 1/12 | 400 Hz |
| 2SS-2 (64 X 64 ELEMENTS / 60 FRAMES/SEC.) | CIIBUXU-X1 | 1800 | 1/8 | 60 Hz |

* DIRECTION OF ROTATION MUST BE CLOCKWISE AS VIEWED FROM SCANNING DISC END OF MOTOR.

Fig. 5. Scanner Wiring Diagram.

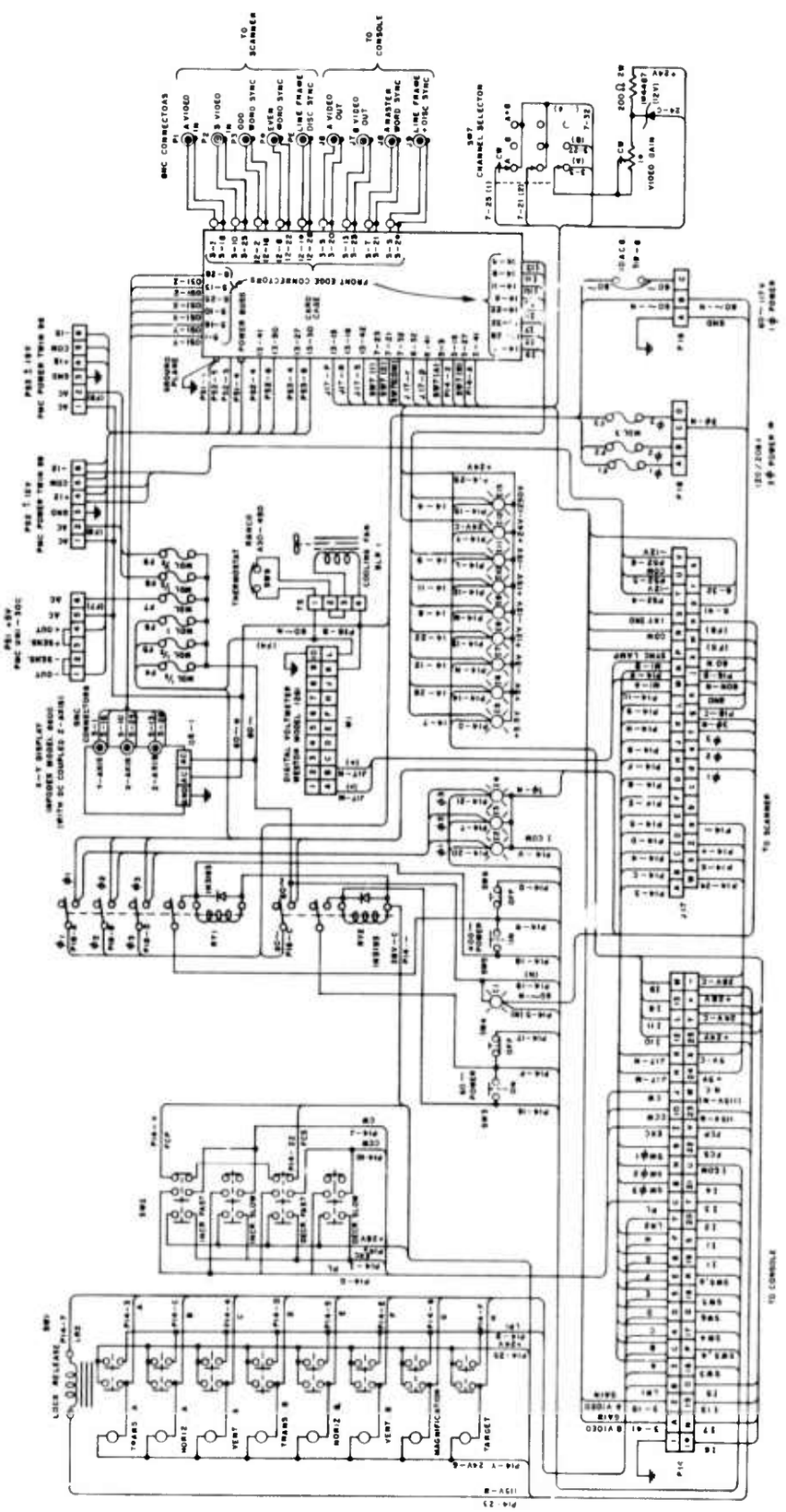


Fig. 6. Scanner Control Unit CU-2 wiring diagram.

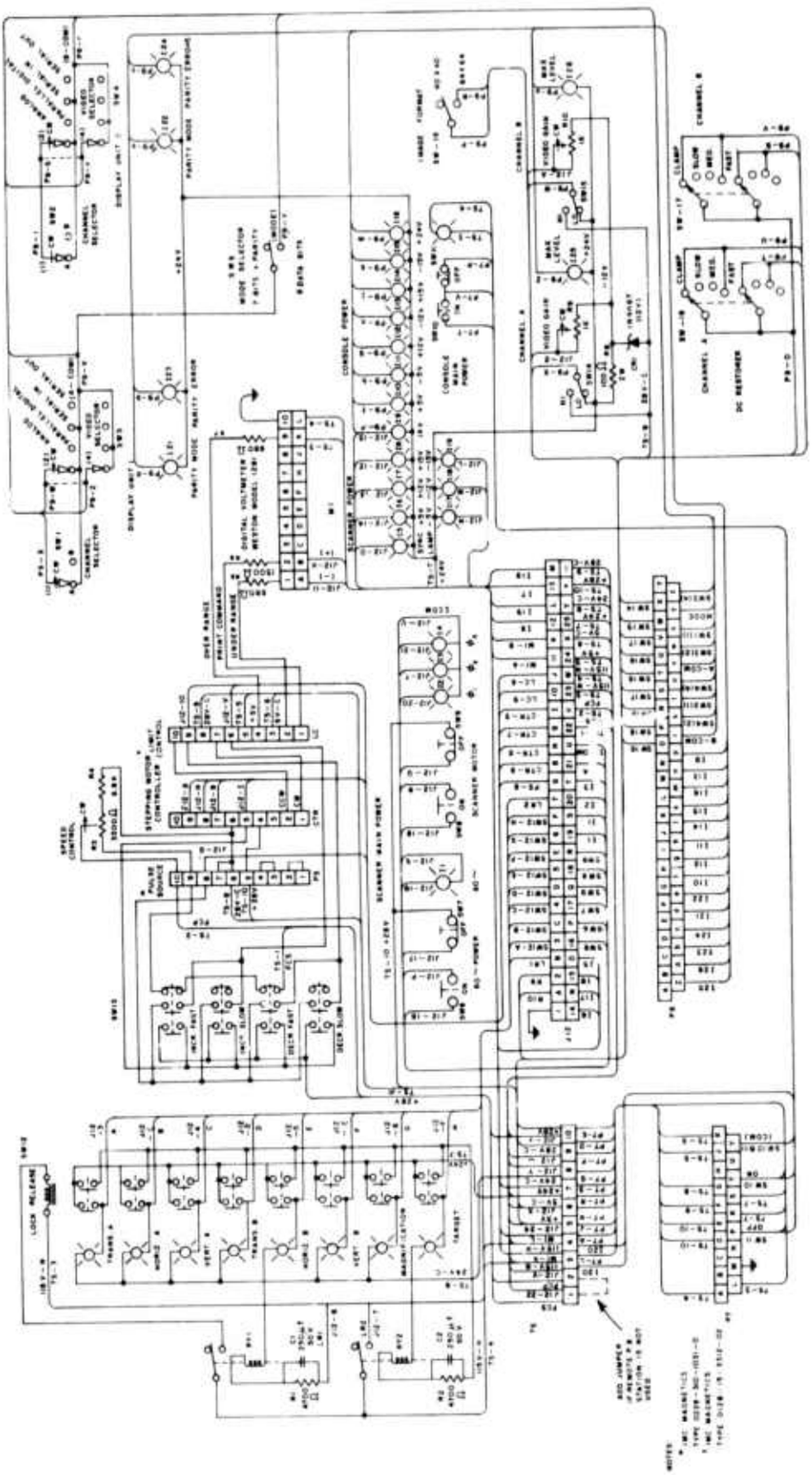


Fig. 7. Console Control Unit CU-1 wiring diagram.

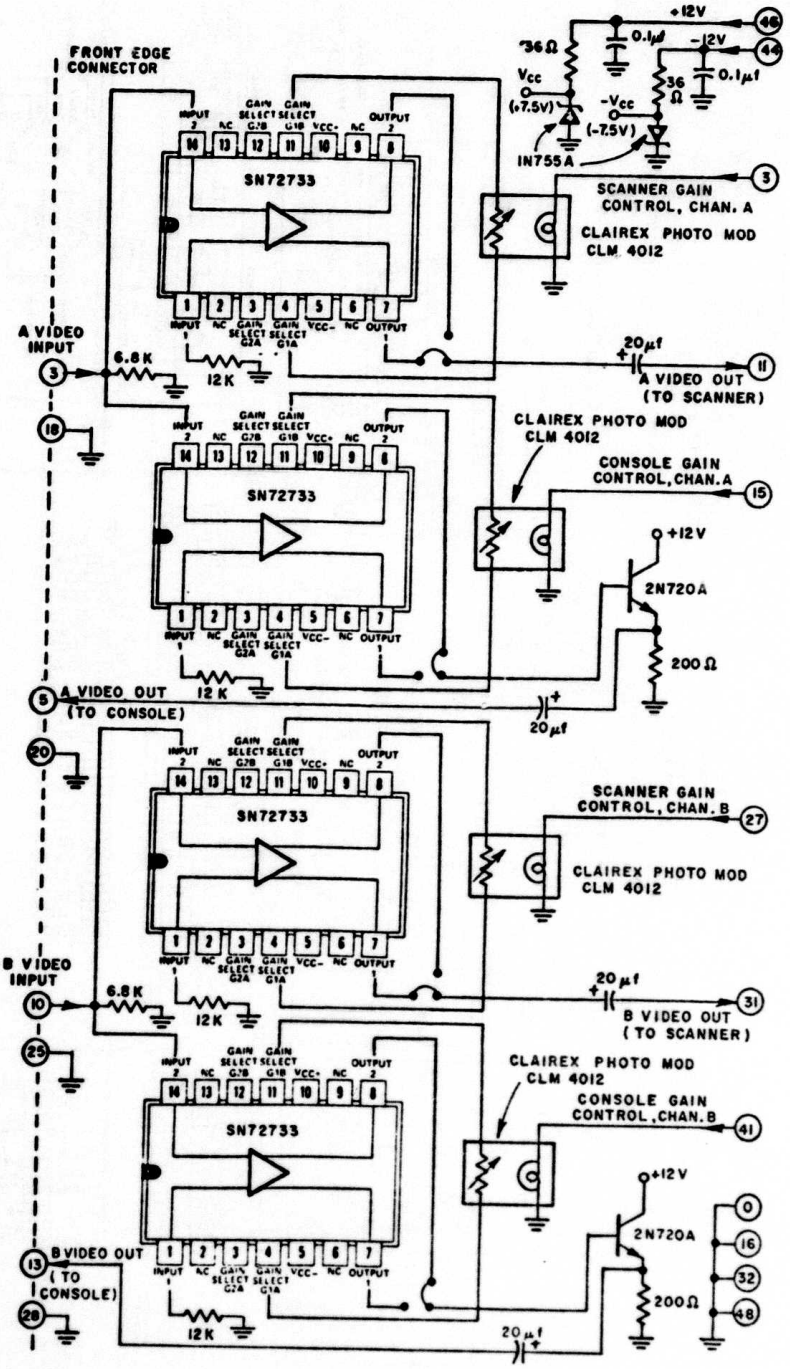



Fig. 8. Video Preamps Schematic Diagram.

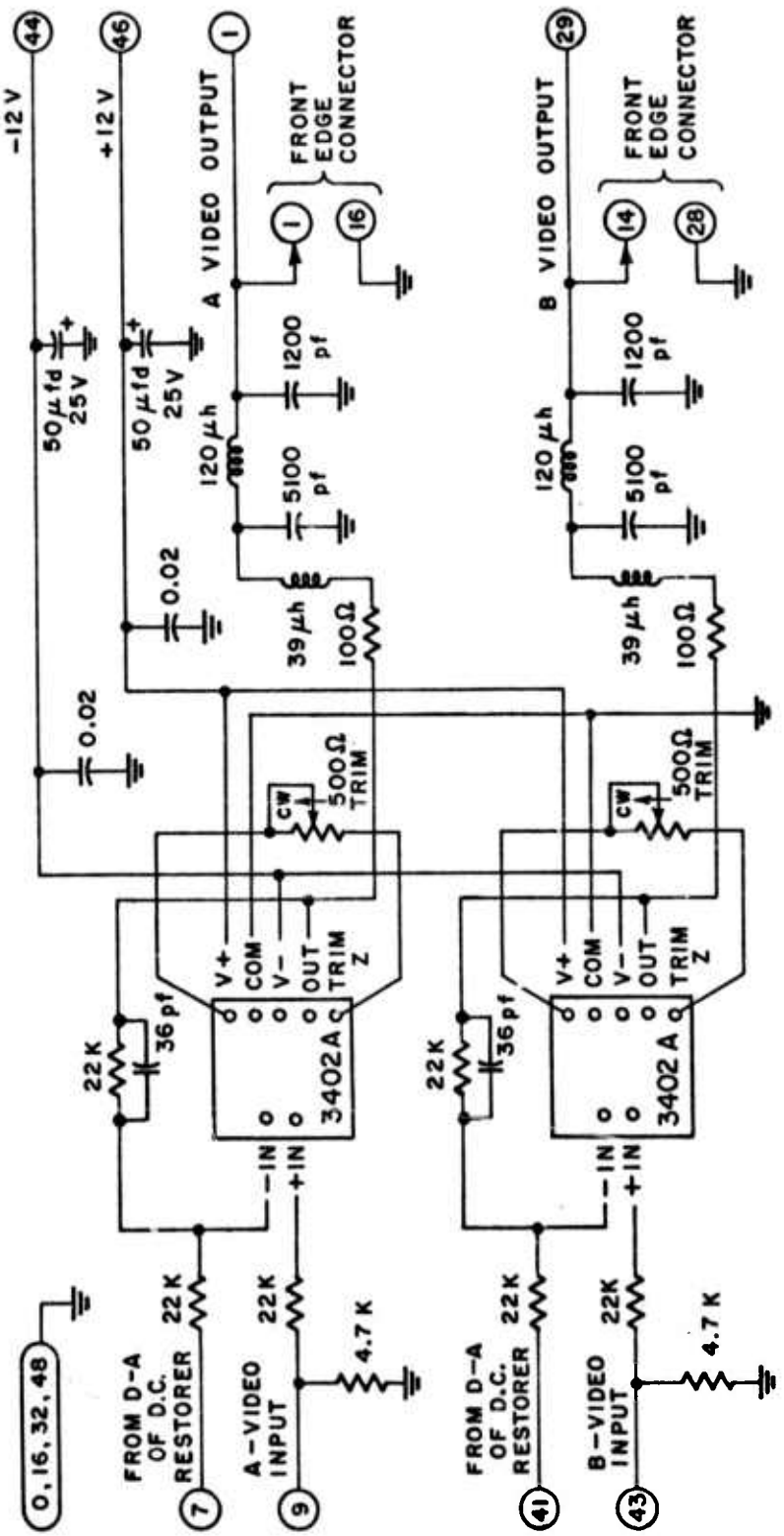



Fig. 9. Video Filters Schematic Diagram.

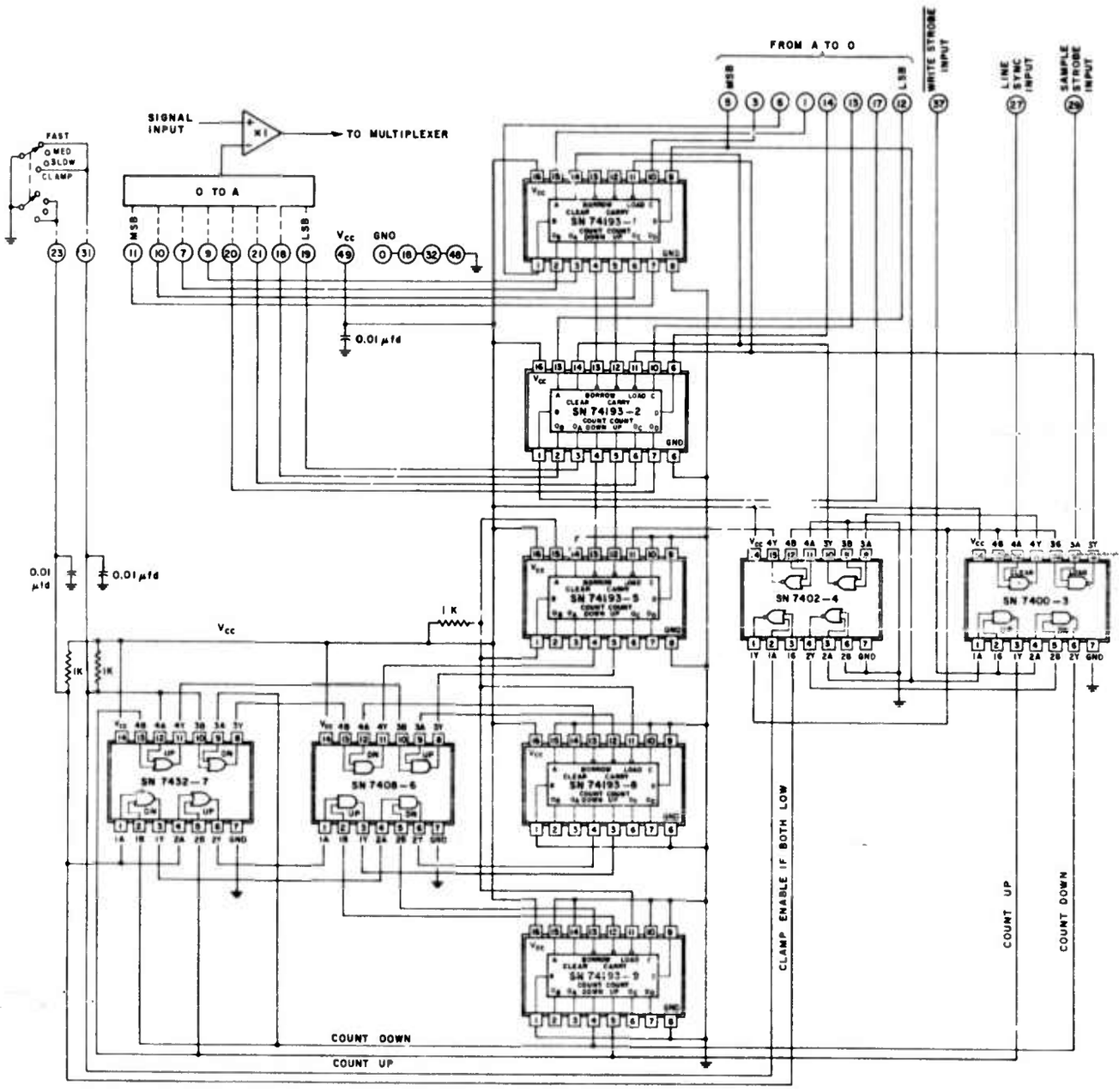



Fig. 10. Digital DC Restorer Logic Diagram.

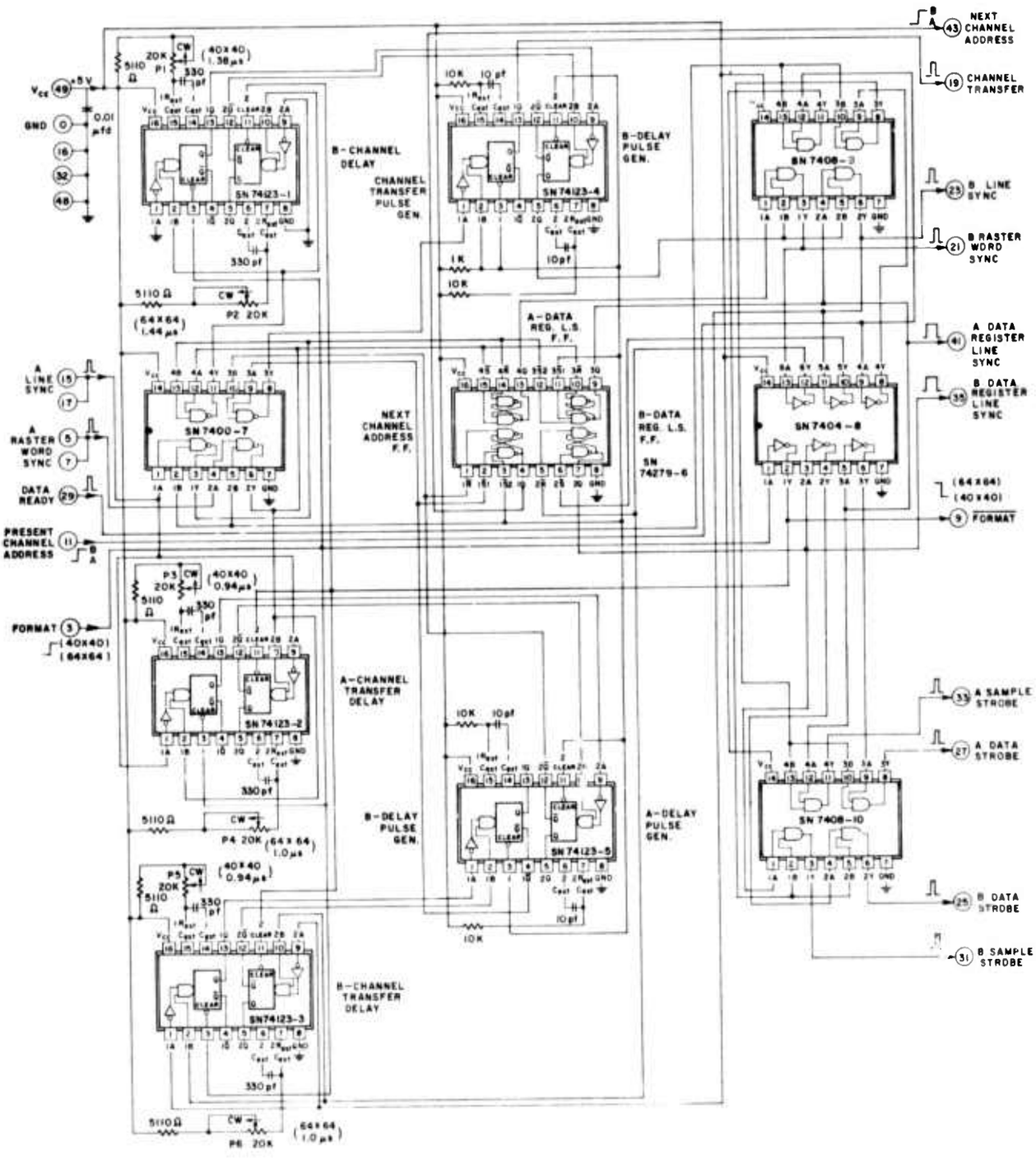



Fig. 11. B-sync Generator and Digital Data Demultiplexer Schematic Diagram.

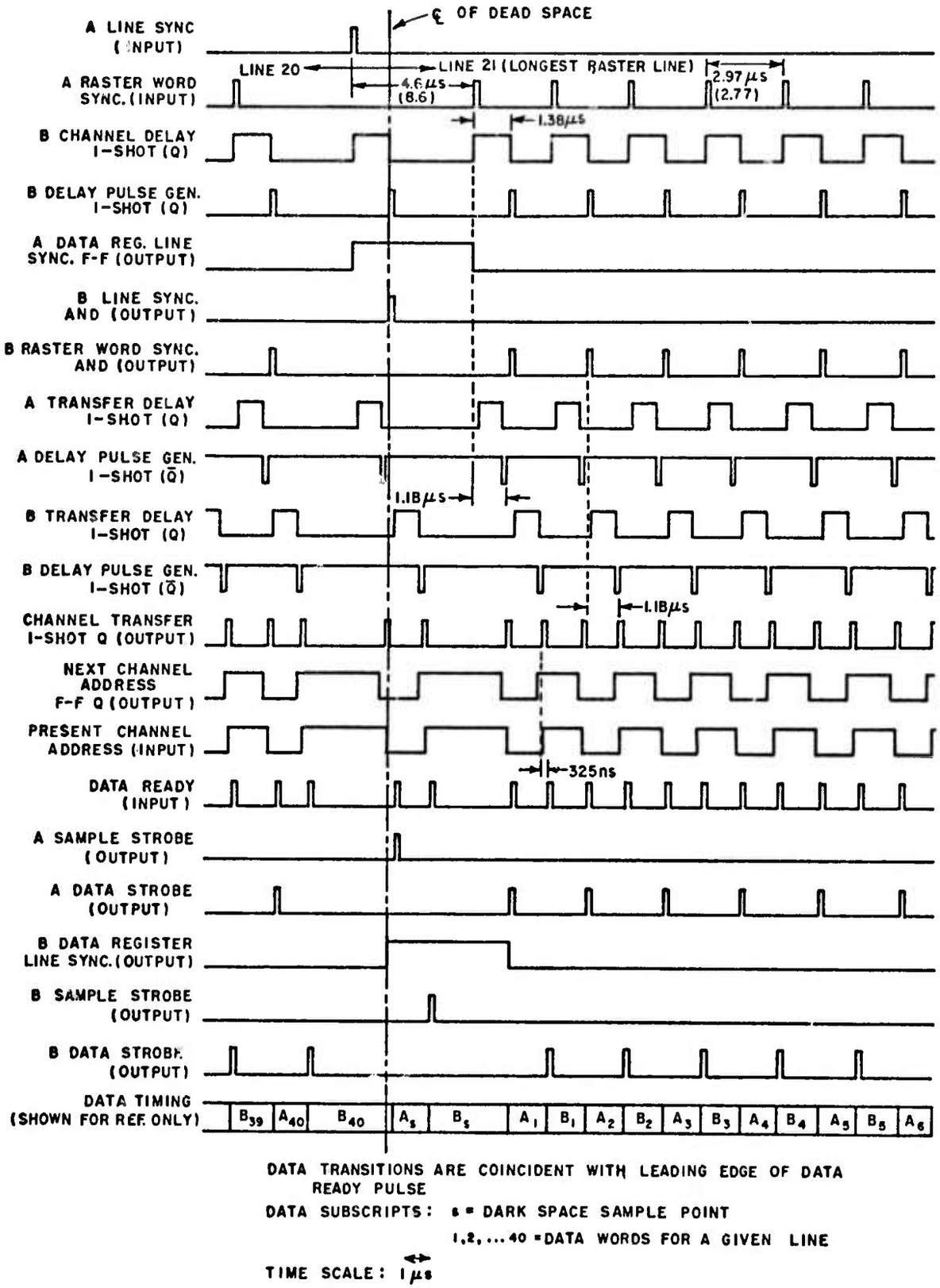



Fig. 12. B-sync Generator and Digital Data Demultiplexer Timing Diagram.

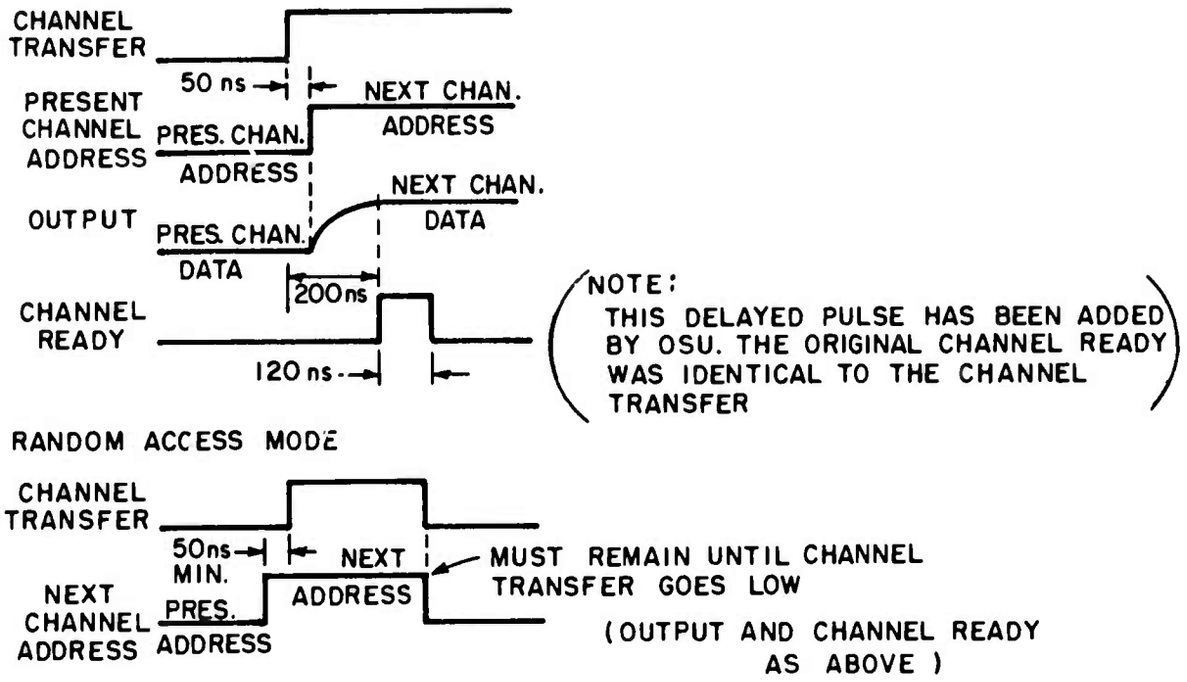



Fig. 13. Multiplexer, MUX-810, Timing Diagram.

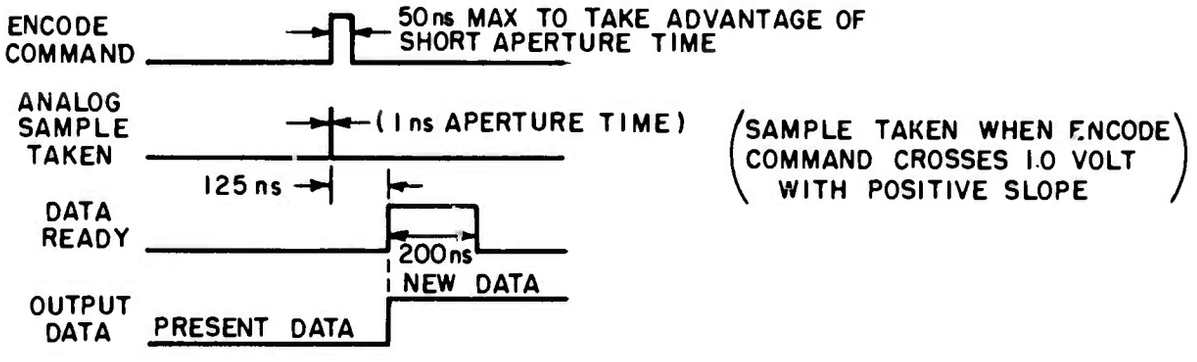



Fig. 14. A/D Converter, HS-802, Timing Diagram.

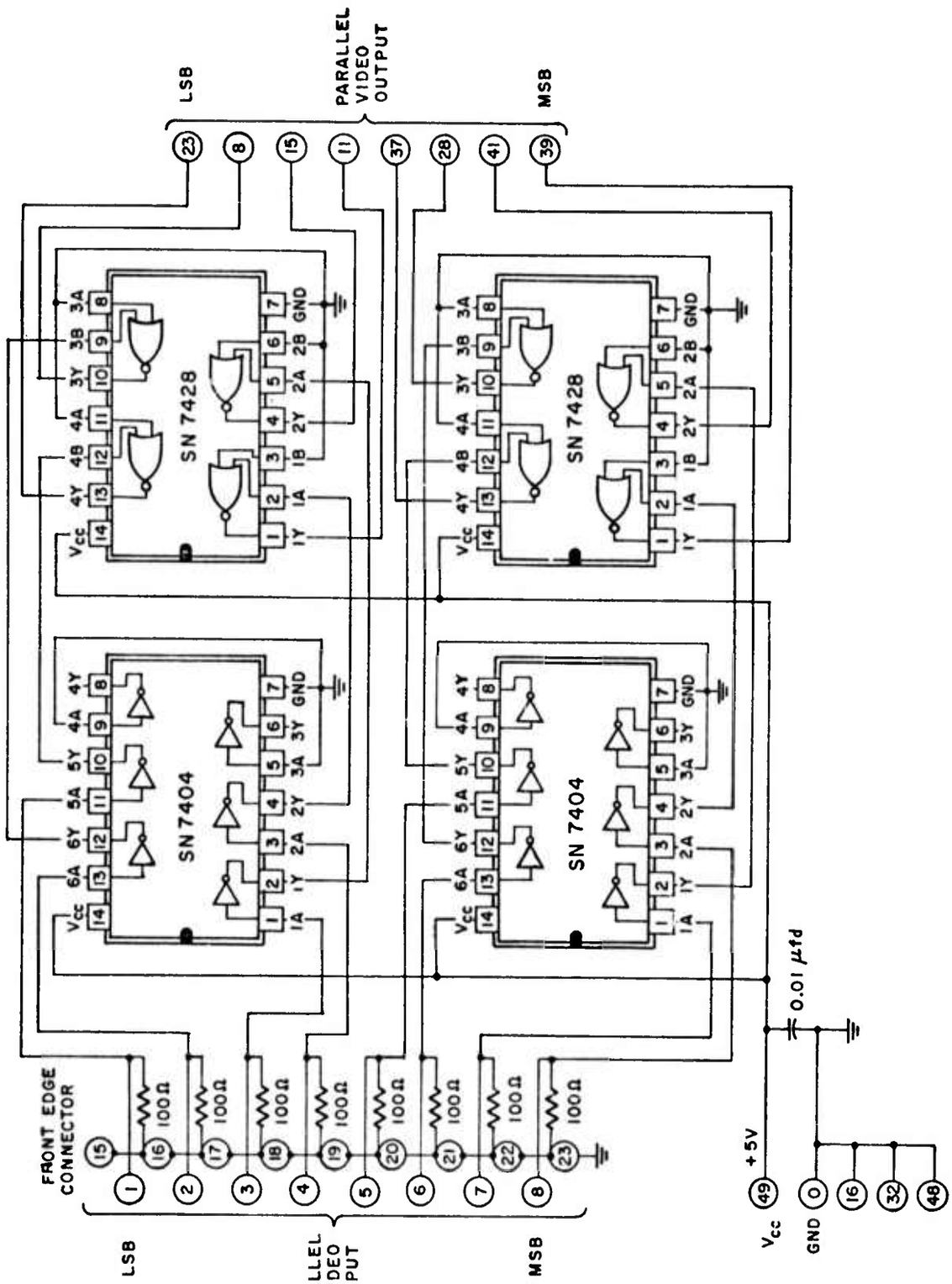



Fig. 15. Digital Video Driver Logic Diagram.

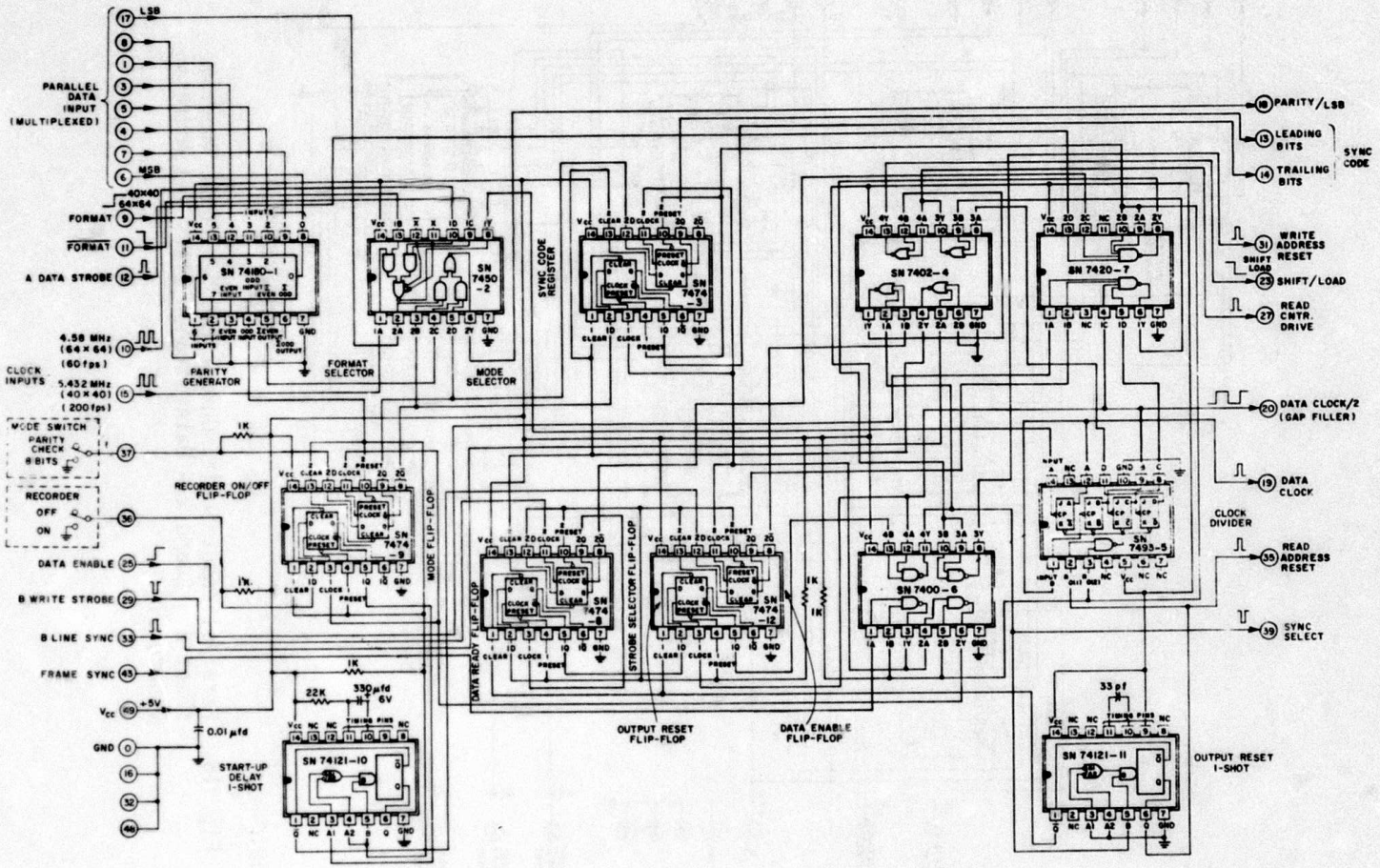



Fig. 16. Parallel Input Serial Output Encoder Logic Diagram.
Sheet 1 - Boarl 1 - control logic.

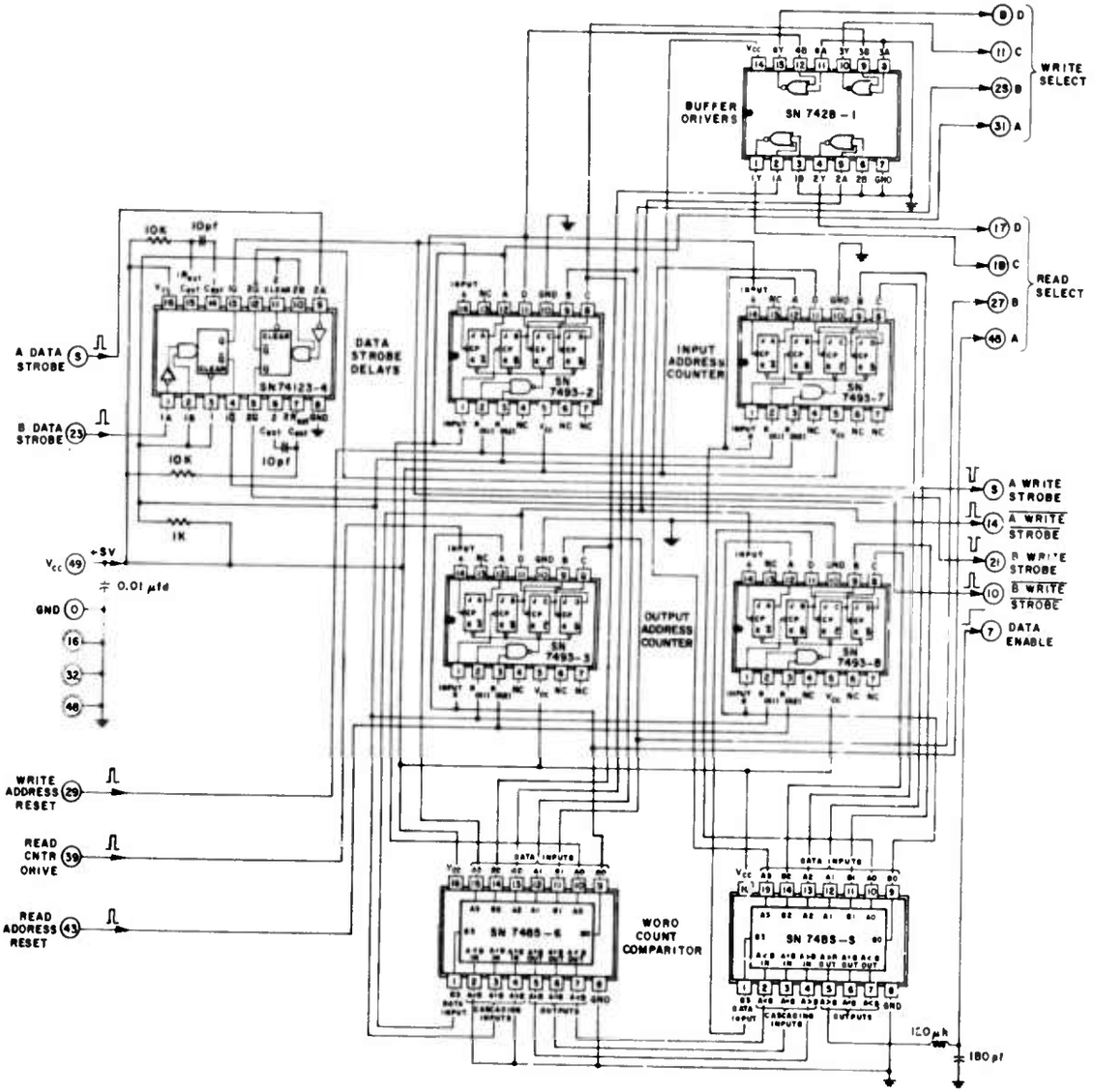



Fig. 16. Parallel Input Serial Output Encoder Logic Diagram. Sheet 2 - Board 2 - Data Strobe Delays and Address Counters.

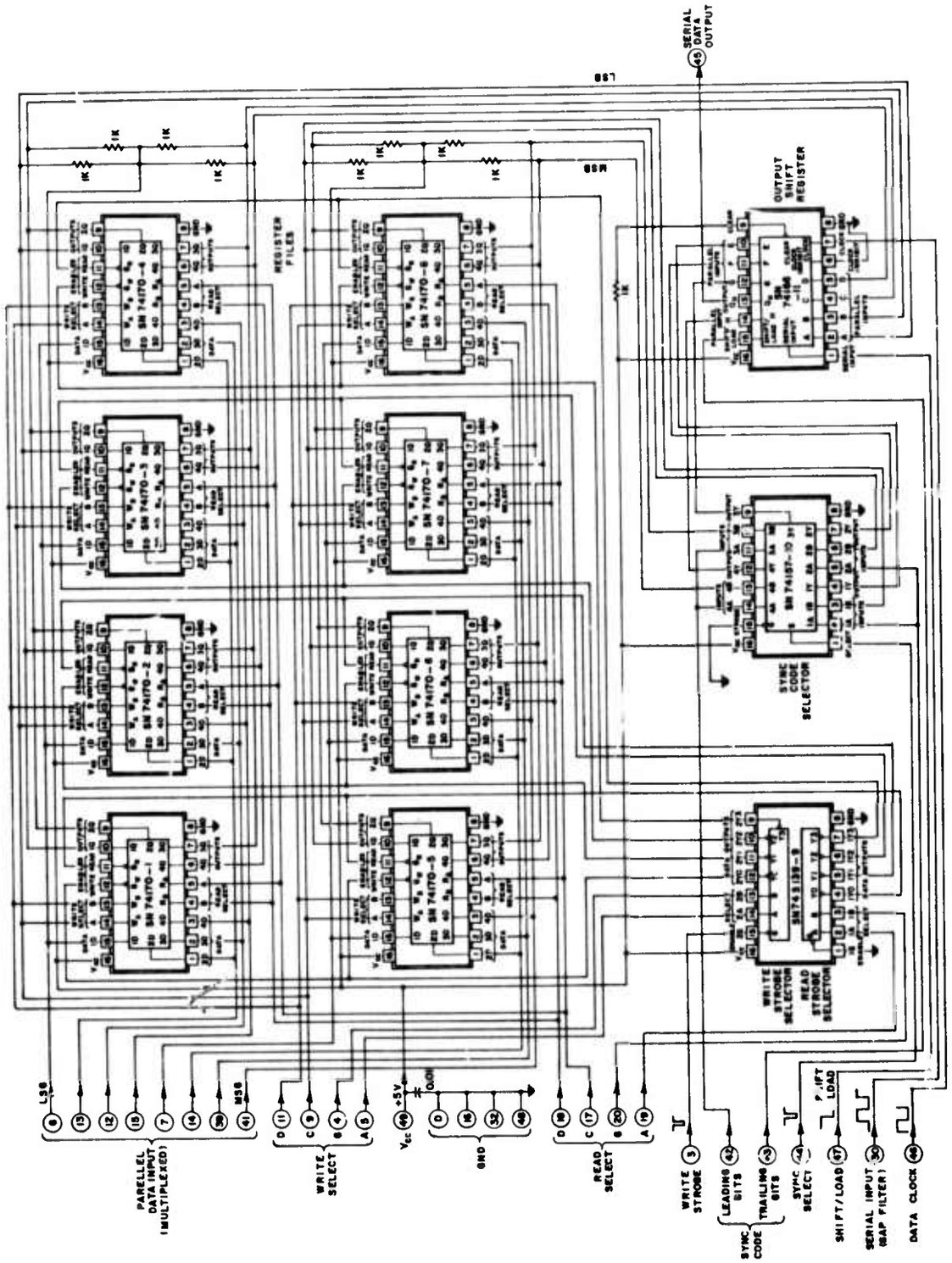



Fig. 16. Parallel Input Serial Output Encoder Logic Diagram.
Sheet 3 - Board 3 - Storage and Output Registers.

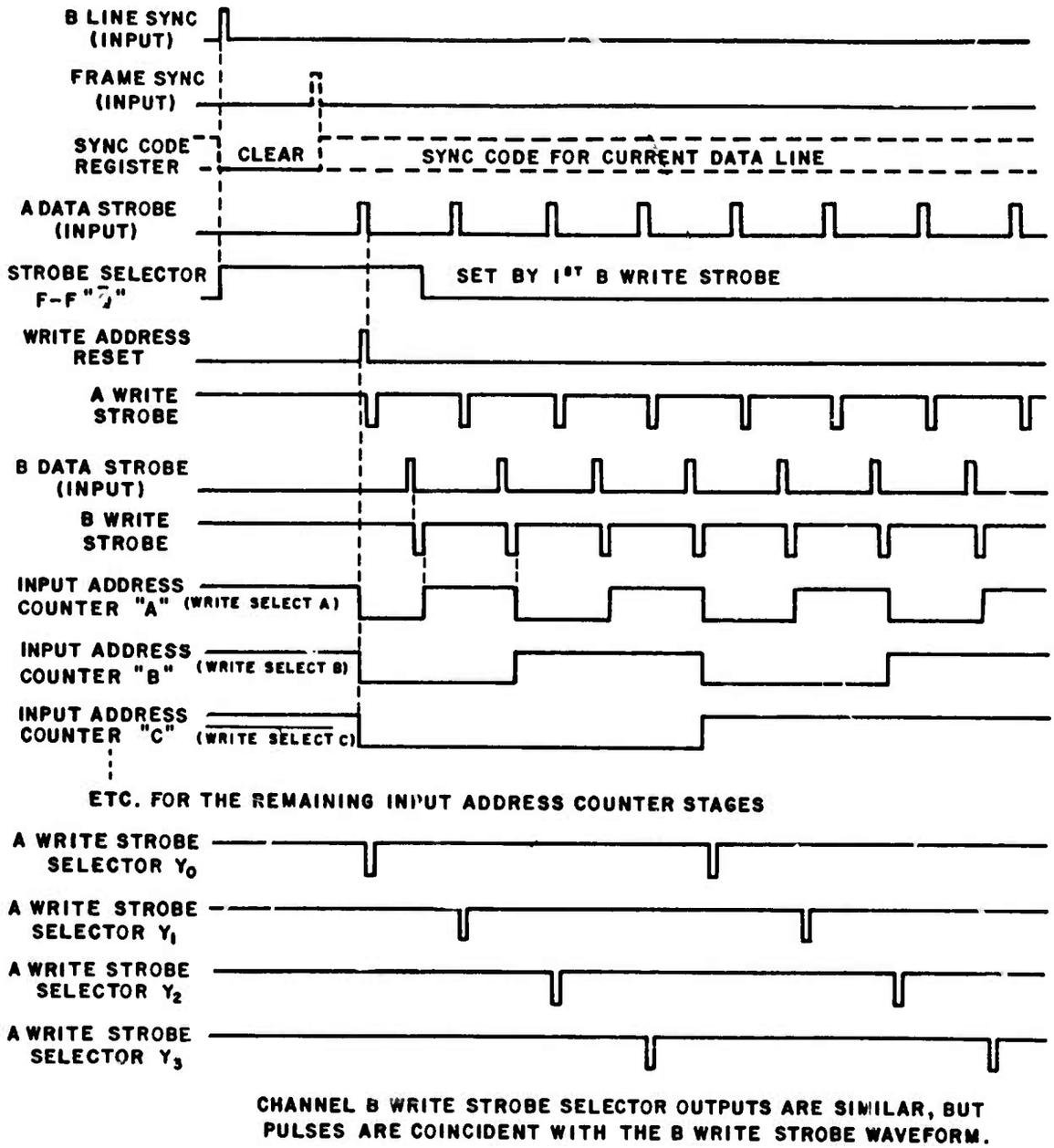



Fig. 17. Parallel Input Serial Output Encoder Timing Diagram. Sheet 1 - Data Input Sequence.

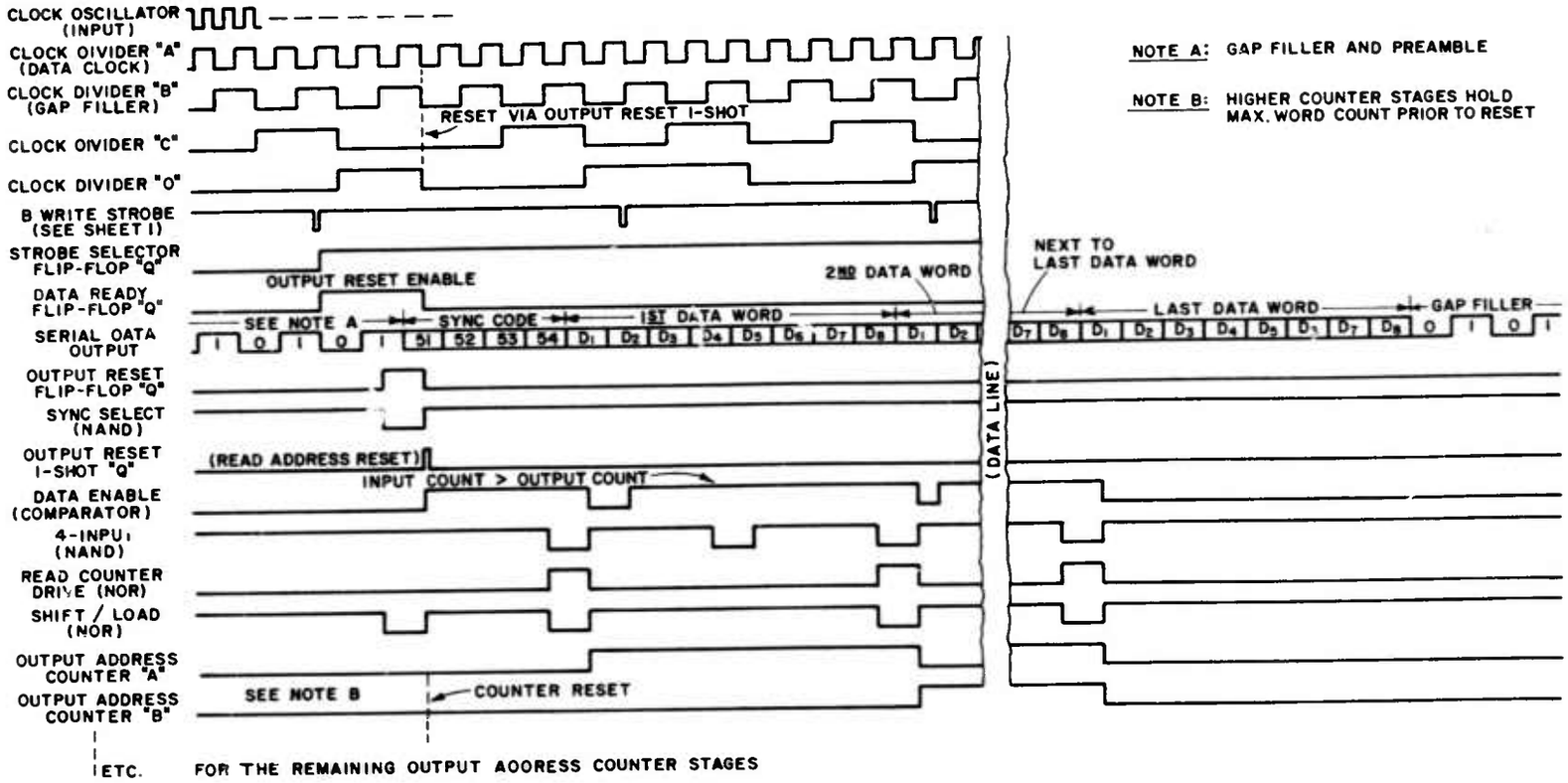



Fig. 17. Parallel Input Serial Output Encoder Timing Diagram.
Sheet 2 - Data Output Sequence.

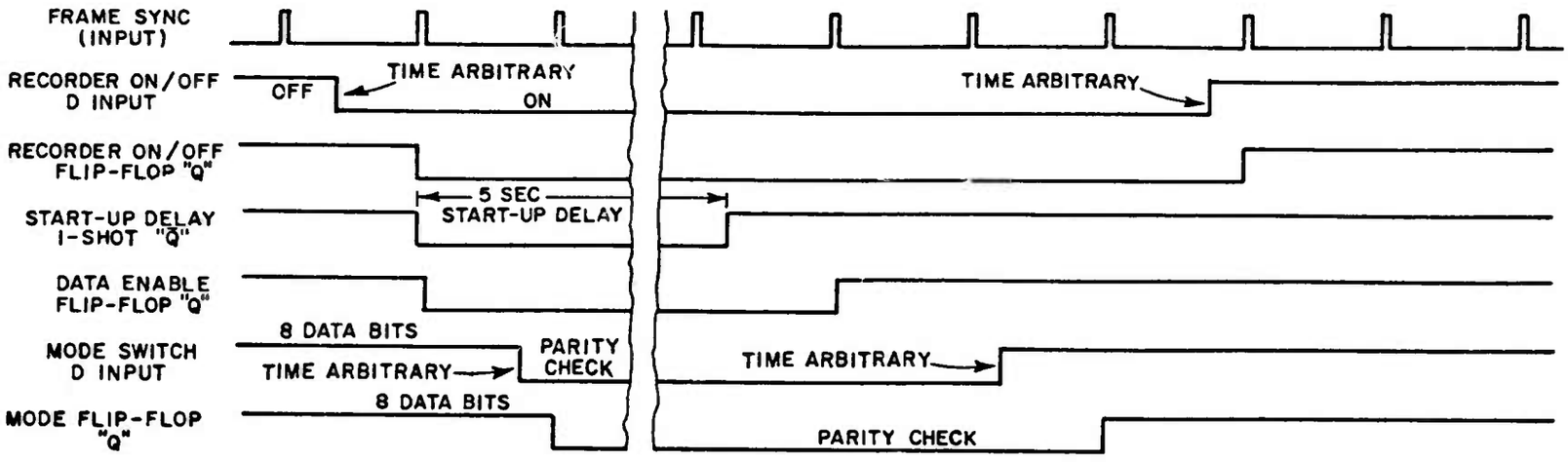



Fig. 17. Parallel Input Serial Output Encoder Timing Diagram.
Sheet 3 - Recorder On/Off and Mode Switching.

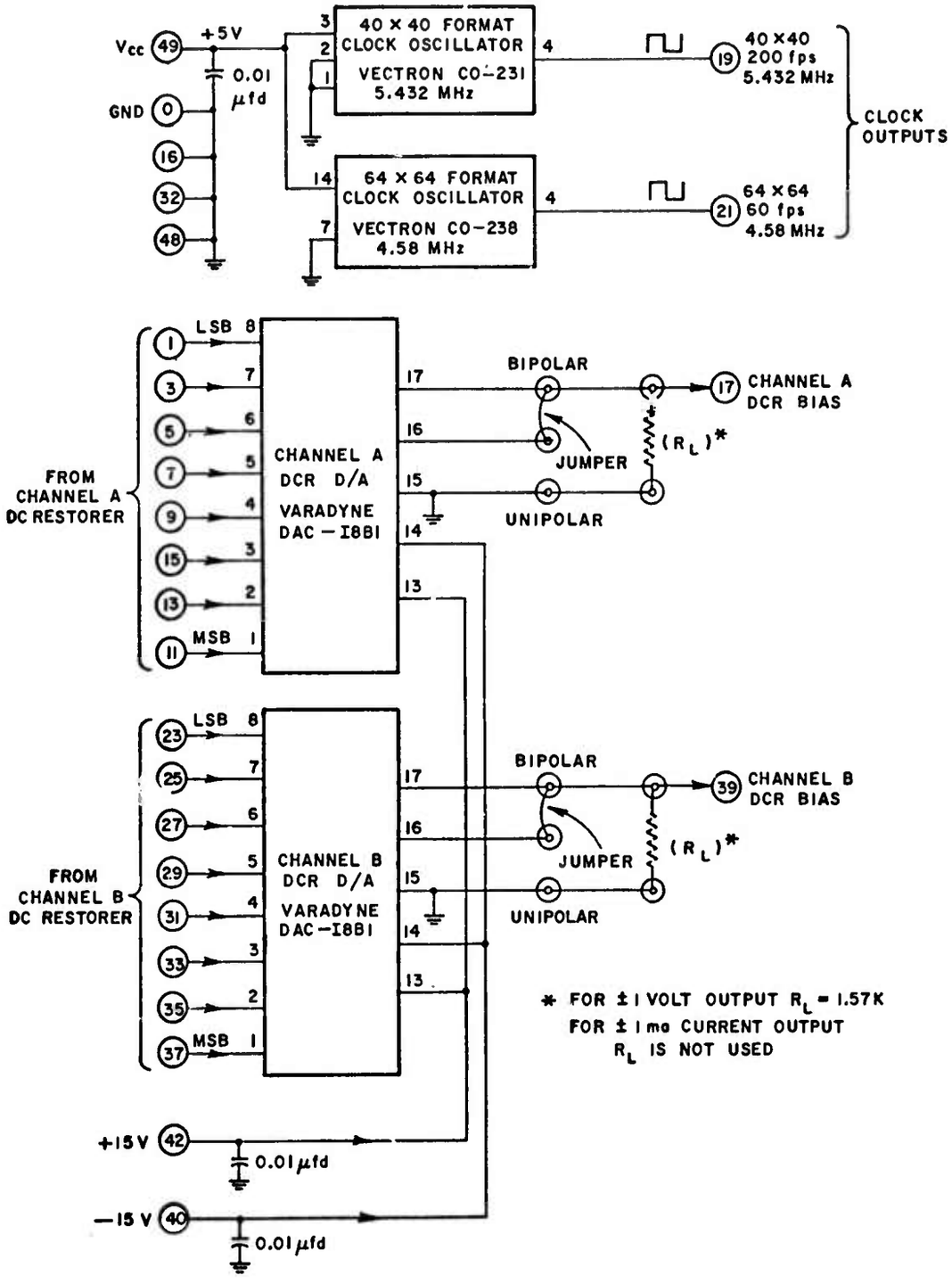



Fig. 18. Data Register Clock and DCR D/A Converters Schematic Diagram.

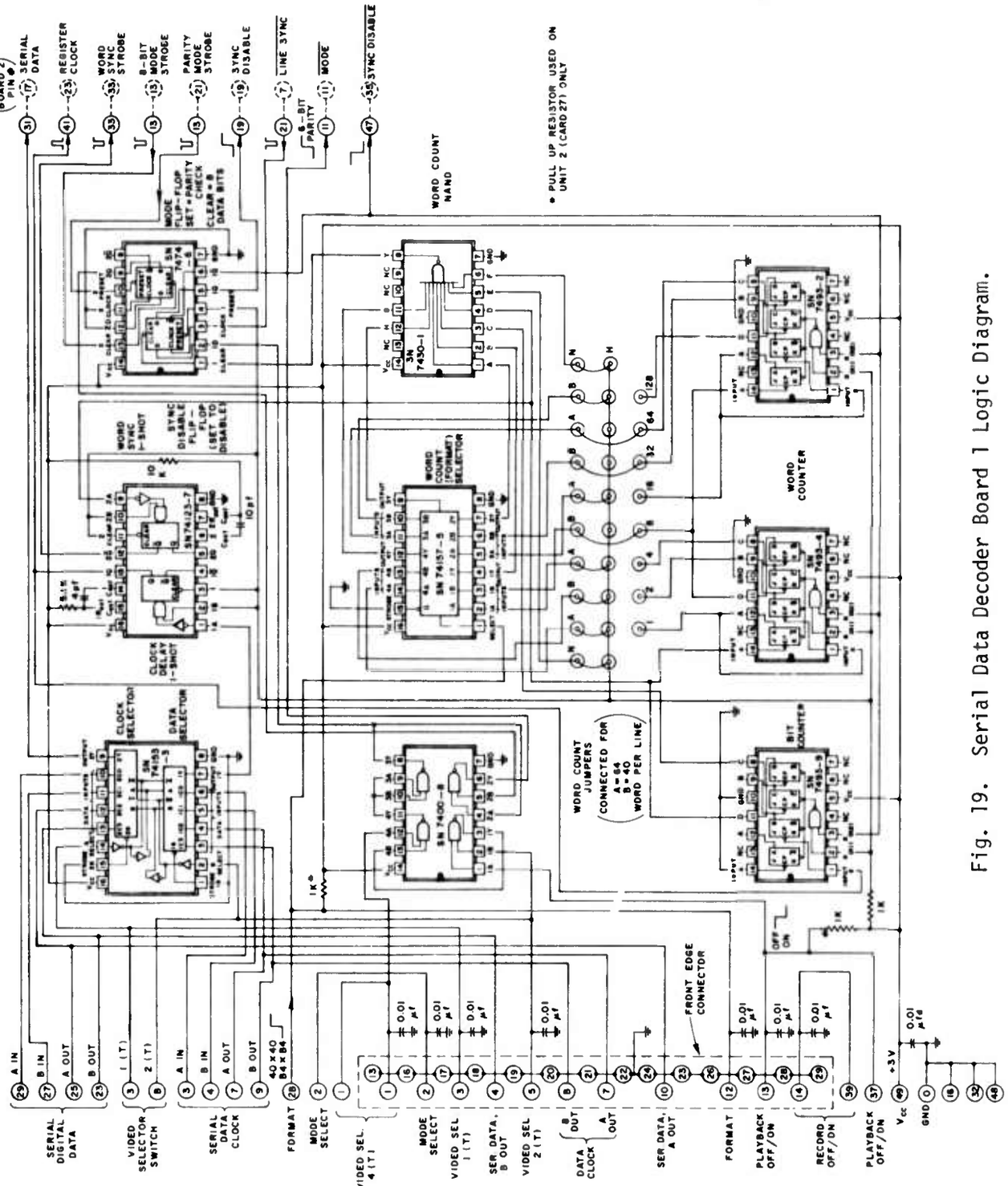



Fig. 19. Serial Data Decoder Board 1 Logic Diagram.

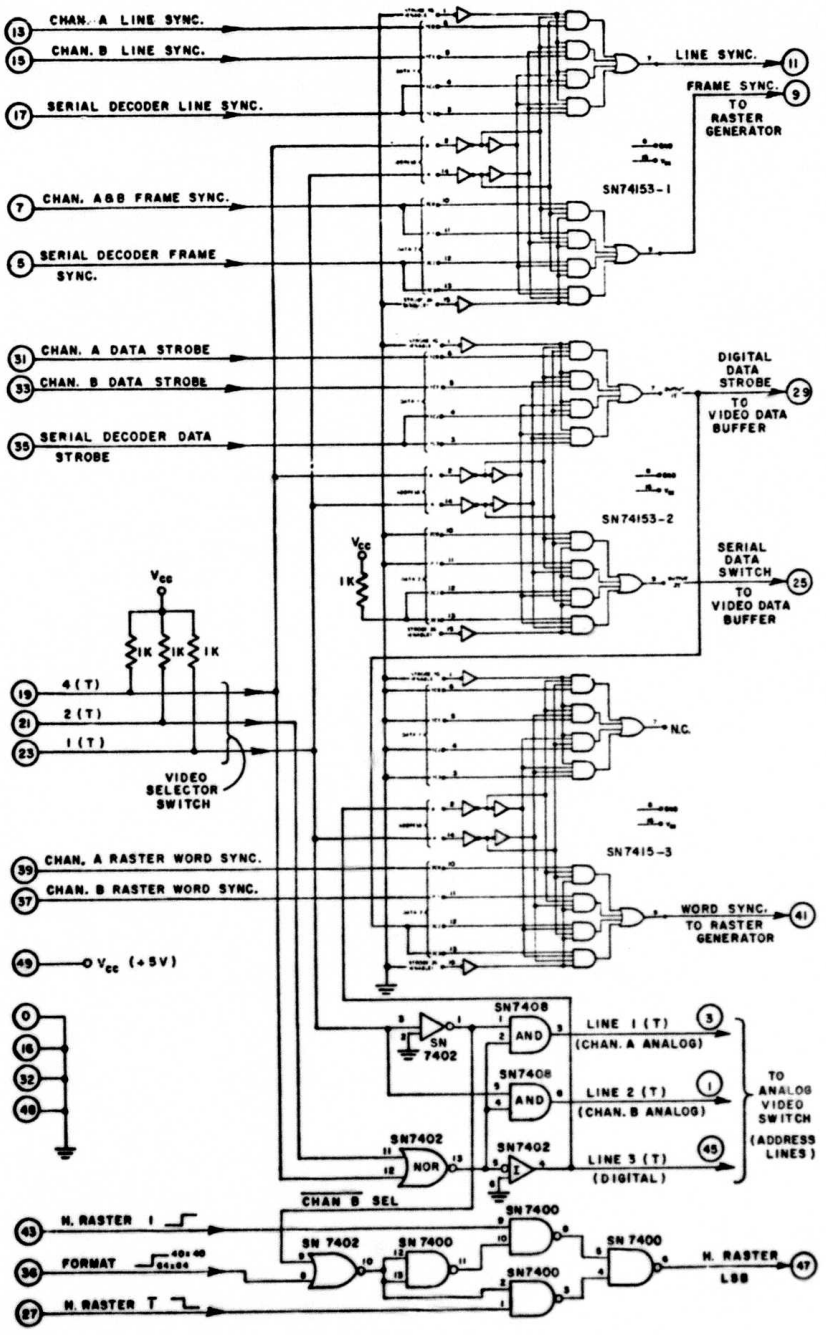



Fig. 20. Video Display Switching Unit Logic Diagram.

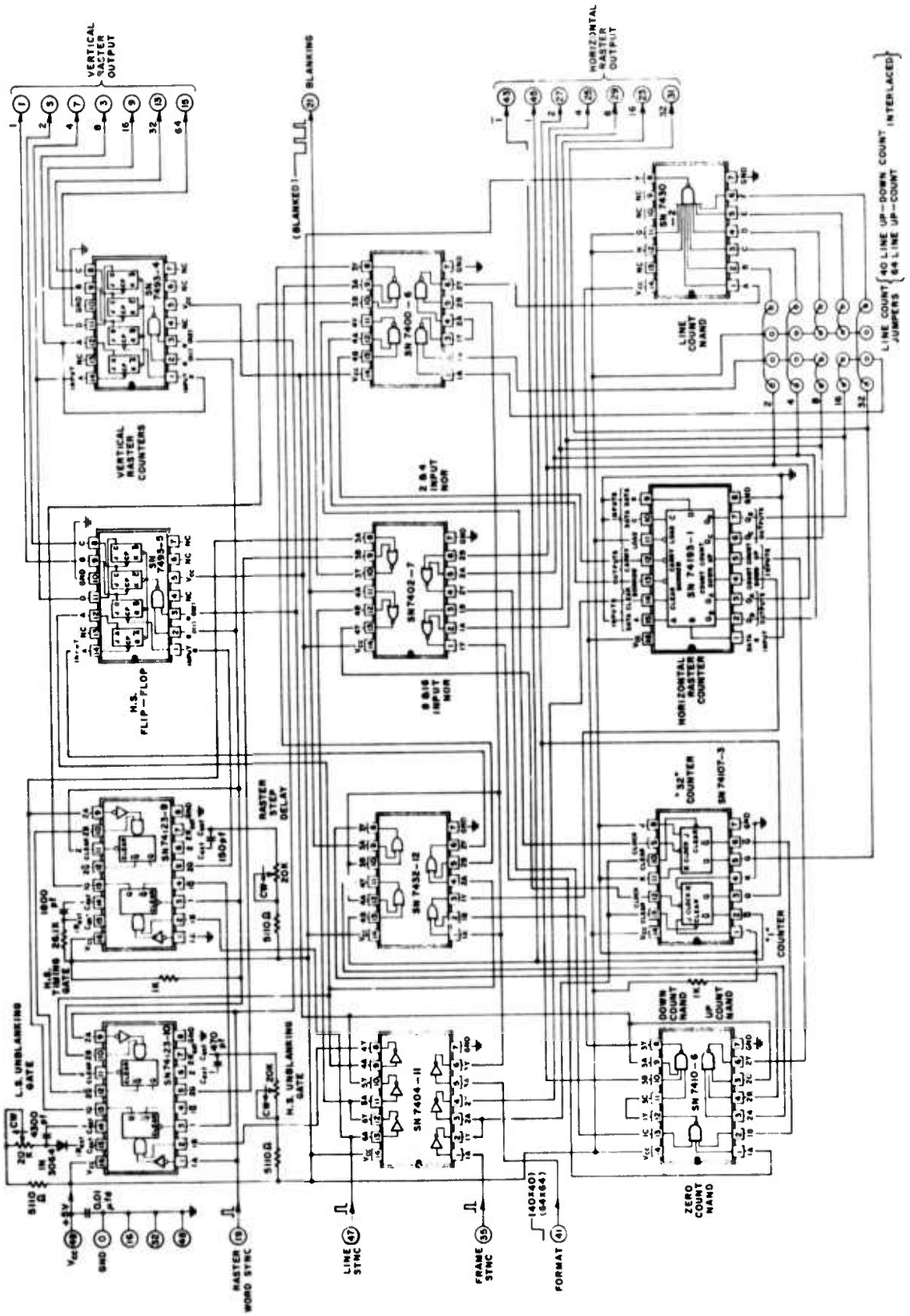



Fig. 21. Raster Generator Logic Diagram.

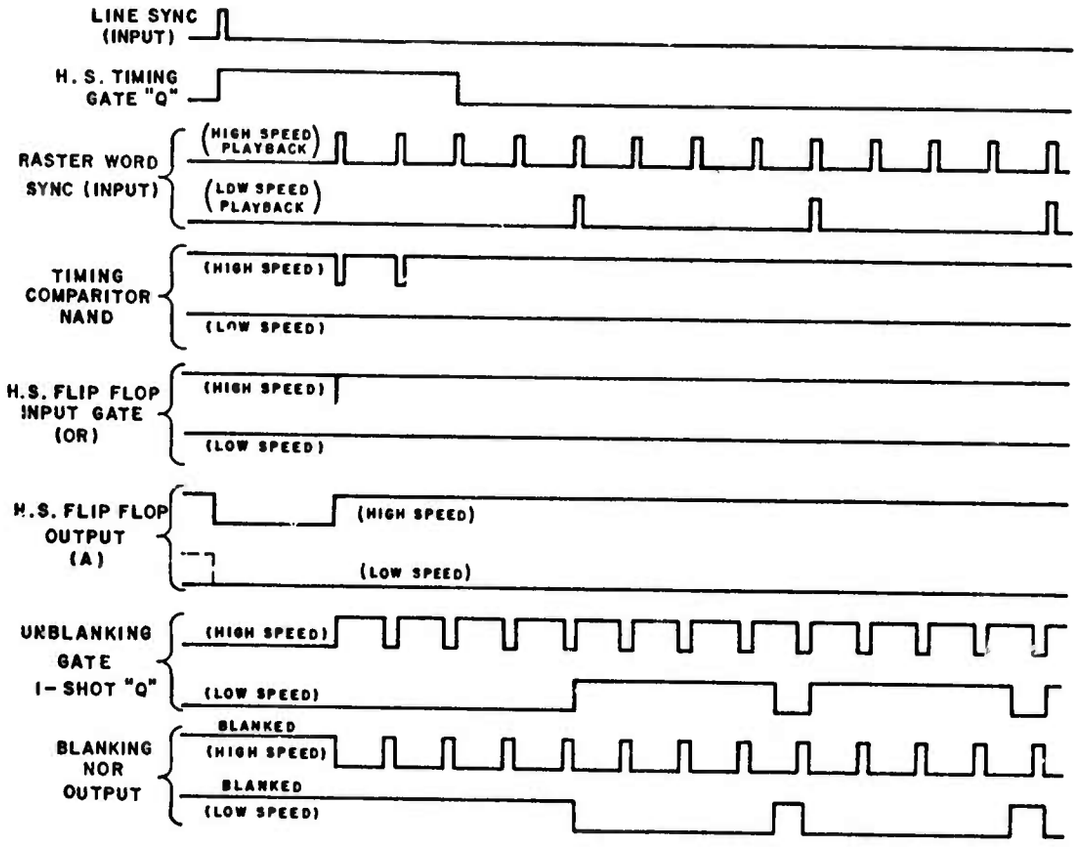



Fig. 22. Raster Generator Timing Diagram.
Sheet 1 - Unblanking Gate
Control Logic.

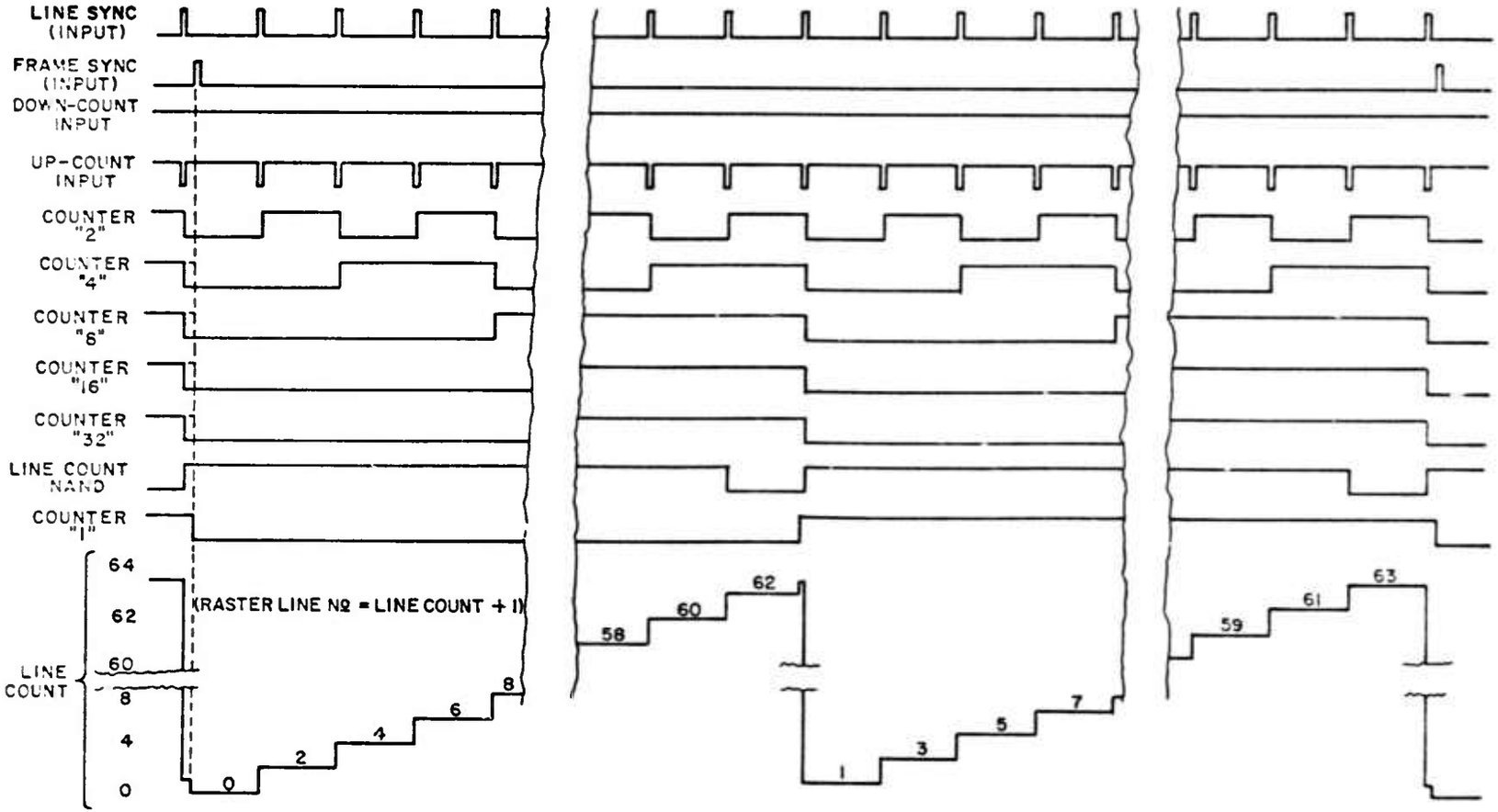



Fig. 22. Raster Generator Timing Diagram.
Sheet 2 - Horizontal Raster
Generator, 64 x 64
Format.

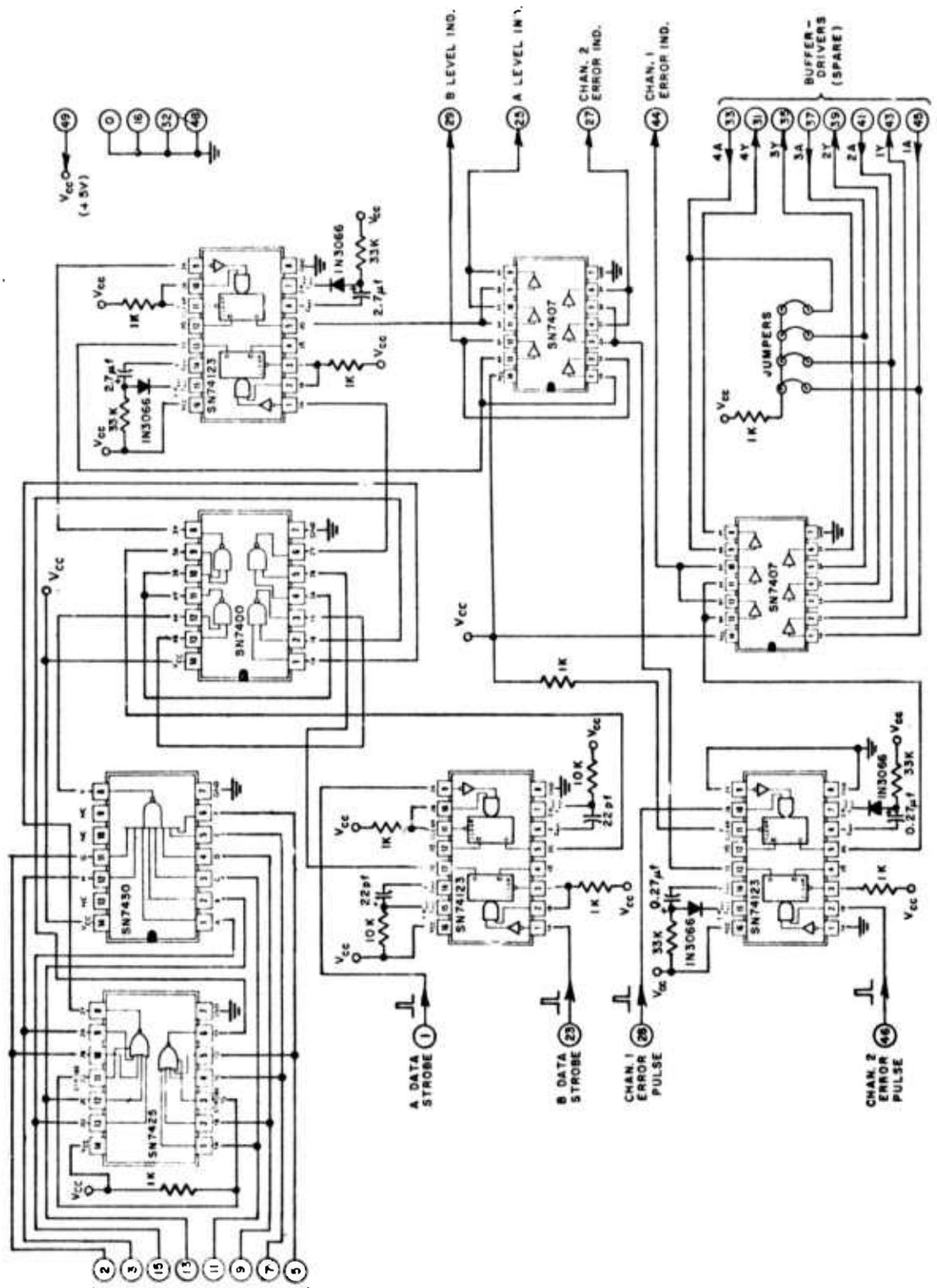



Fig. 23. Video Level and Error Indicators Logic Diagram.

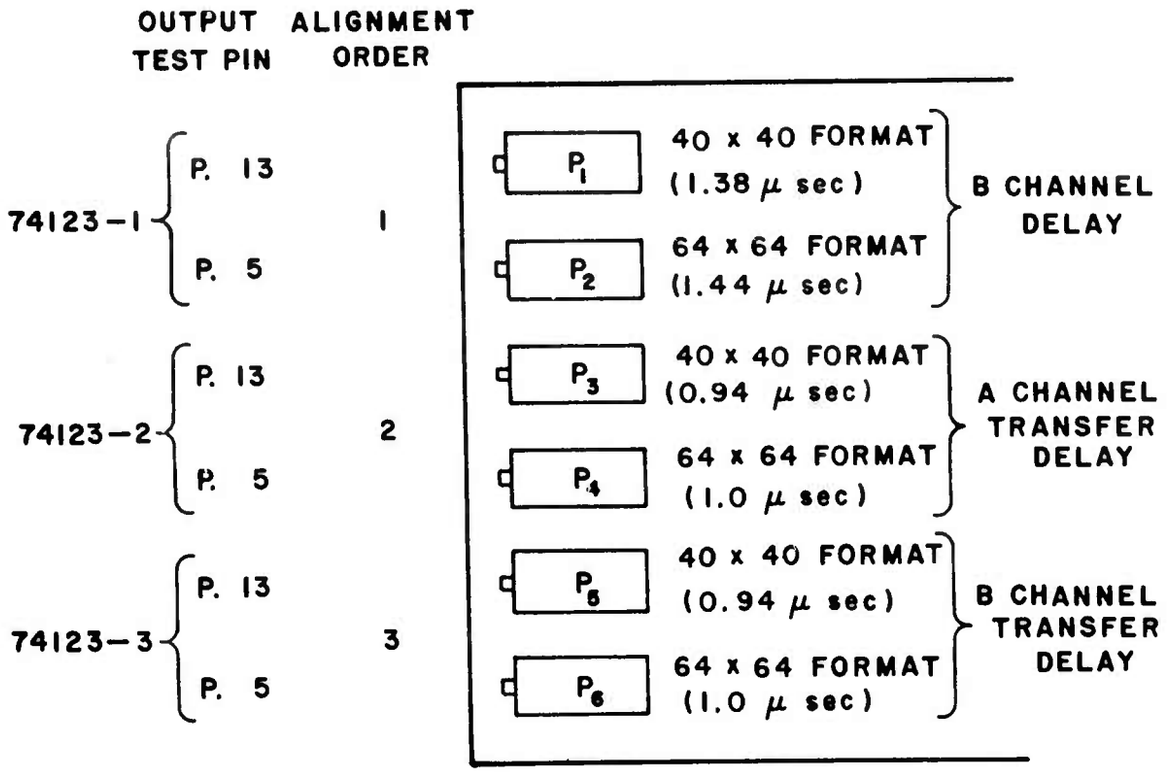



Fig. 24. B-sync Generator Control Locations.

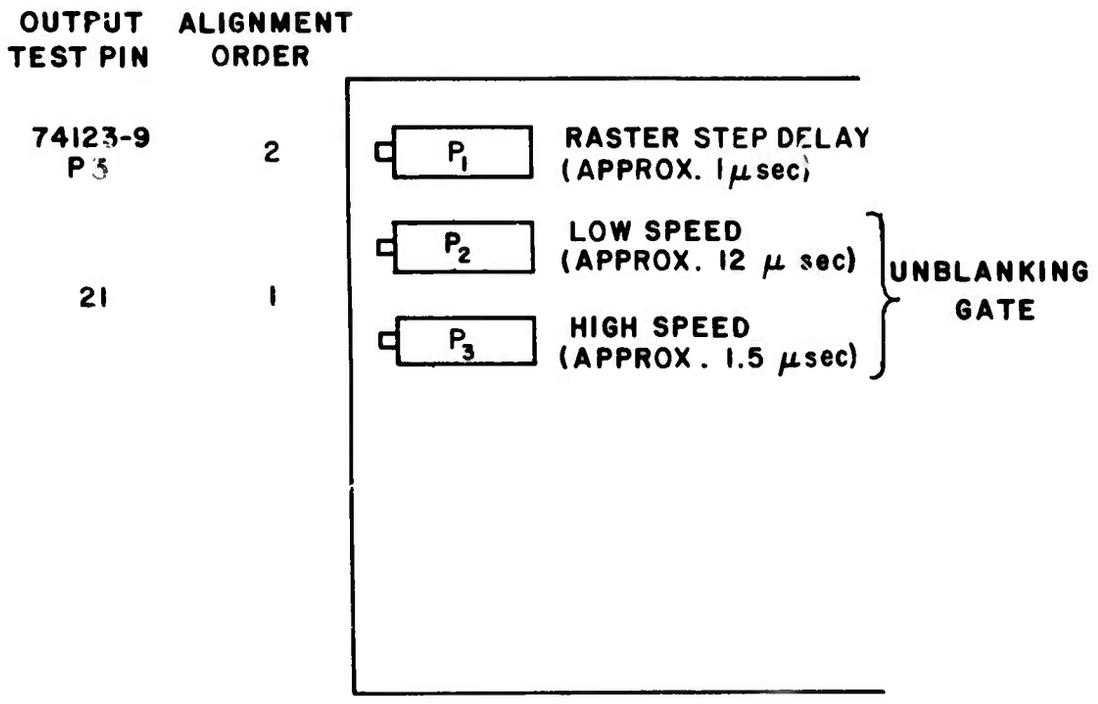



Fig. 25. Raster Generator Control Locations.

# APPENDIX II
# IR SCANNER ALIGNMENT AND MAINTENANCE

Alignment and maintenance procedures for the modified scanner system generally parallel those previously given in Ref. 1, APPENDIX IV. In particular, Section A., General Maintenance Procedures, given in that Appendix, should be studied before any attempt at system realignment is made.

Alignment of the sub-assembly and electronics for the 40 x 40 element, 200 frames per second image format remains the same as given previously (Ref. 1), except that the physical locations of some of the adjustment potentiometers have been changed (See Figs. 24 and 25) as a result of necessary changes in circuit board layout and card cage locations to accommodate the new image format. Changes in the maintenance and alignment procedures as given in Appendix IV, Ref. 1, including those applicable to the 64 x 64 element image format are given below. (Page and paragraph numbers refer to Appendix IV, Ref. 1).

| Page and paragraph | change required |
|---|---|
| p. 145, A. (3rd paragraph) | Drill diameter for the 64 x 64 element format scanning disc apertures is 0.005 in. rather than 0.008 in. as used for the 40 x 40 element format disc. Because of the smaller hole diameter and thinness of the material, this cleaning procedure is not recommended for the 64 x 64 element format disc. |
| p. 145, A-1-a. | The 60 sec. off cycle to reset the 5.5 volt power supply is no longer required since this power supply has been replaced. |
| p. 146, A-2-b. (2nd paragraph) | Sixty-four output pulse trains (32 pulses per train) corresponding to 64 successive data lines should be viewed (i.e., 1 complete rotation of the scanning disc) for the 64 x 64 element format. |
| pp. 146-7, A-3 | A 60 Hz 3-phase supply is used for the scanner motor, 64 x 64 element format, consequently 60 Hz Hum modulation, rather than 400 Hz should be observed. |
| p. 147, B-5 | A GE Type 1493, 6.5 volt lamp is used in each sync projectors of the 64 x 64 element format scanner sub-assembly. |

p. 148, C-2-b

Oscilloscope sync for waveform observation when the 64 x 64 element image format is used should be frame sync (since disc sync is not used with this format). Frame sync may be obtained from TP4 of the scanner control unit card cage, or pin 5-23 of the console control unit card cage.

p. 149, C-2-d

Disc sync is not used with the 64 x 64 element format (see above). Use of the delayed sweep is still required, however, since line sync precedes frame sync.

p. 150, C-2-g

Use frame sync (TP4) for the 64 x 64 element format (see above).

p. 151, C-3-b

Relative timing between line and frame sync pulses, and between frame sync and the first word sync pulse, should be approximately 5 μs for the 64 x 64 element format. Disc sync is not used for this format, as stated above.

p. 152, C-4

The B-sync generator now contains six alignment controls, three for each format, which are to be adjusted as specified when the associated scanner sub-assembly is installed and in operation. Control locations and order of adjustment are given in Fig. 24 of this report which replaces Fig. 67 of Ref. 1.

pp. 152-3, C-5-a

Separate unblanking gate adjustments are now used for high and low speed displays (see Chapter II-B and IV-C-13). The high speed unblanking gate may be adjusted during real time display with the scanner in operation as specified previously (Ref. 1). The low speed unblanking gate must be adjusted (in similar manner) during slow speed playback of a pre-recorded tape (with display indicator selector set to the "serial out" position). Proper adjustments of these controls should be compatible with both image formats. Note that the settings for both image formats (console displays only) may be checked using pre-recorded tapes regardless of which scanner sub-assembly may be installed as previously described in Chapter III-B-2-b of this report.

Control locations for the new master generator boards are given in Fig. 25 which replaces Fig. 68 of Ref. 1.

p. 154, C-6-a

Angular position of the splitting mirror edge is 2.8125° ccw from vertically downward for the 64 x 64 element scanner sub-assembly.

p. 154, C-6-c, (1)

Use frame sync (TP4) for the 64 x 64 element image format.

p. 154, C-6-f-1

For the 64 x 64 element format, word sync pulses for a line elsewhere in the frame (rather than the first line) will be first to drop out as the reticle is raised. Find this line (using a slow sweep speed) and then view this line (using expanded, delayed sweep) for the adjustment procedure described.

p. 155, C-6-j-1

A frame for the 64 x 64 element format contains 64 lines.

p. 155, C-6-j-4

For the 64 x 64 element format scanner sub-assembly hole No. 64 should scan the top line and hole No. 1 should scan the bottom line of the word sync reticle.

p. 156, C-7

Disc sync is not used for the 64 x 64 element format scanner sub-assembly, hence there are segments for only frame sync and line sync on the corresponding sync reticle. The line sync portion of the reticle is divided into two line segments, however, in order to achieve an essentially constant time interval between the line sync pulse and the first word sync pulse of each data line. (The 40 x 40 element system uses a single line segment for the line sync reticle giving a variable time interval for different data lines because of the scanning method used - see Chapter III-B-3.)

The two-segment line sync reticle causes some difficulty during alignment since an incorrect vertical (and/or rotational) adjustment of the reticle can cause a single scanning aperture to scan a part of each line segment producing two pulses spaced in time similar to those normally produced by the line sync and frame sync pulses. An extraneous frame sync pulse is generated under these conditions by the sync separator, interferring with oscilloscope (and display indicator) sync thus making proper adjustment difficult. Hence, throughout the alignment procedure, it is necessary to use particular care to insure that only the proper frame sync

pulse is generated and used for syncronization purposes. One way to check this is to temporarily cover the frame sync portion of the projected reticle (with a piece of cardboard, screw driver blade or other suitable instrument). Loss of sync with the reticle thus shielded is a good indication that proper frame sync was being used.

p. 156, C-7-b-1 — Proper projected reticle size (and vertical position) for the 64 x 64 element format scanner sub-assembly is obtained when the frame sync aperture is centered in the corresponding frame sync reticle segment and when the break in the line sync reticle occurs between scanning apertures No. 48 (just above the break) and No. 17 (just below the break).

p. 156, C-7-c — No disc sync is present for the 64 x 64 element format. Timing between the line sync and frame sync pulses should be approximately 5 μs (not critical). Rotation (and vertical adjustment) must be such that no extraneous frame sync pulses are produced. (see C-7, above).

p. 156, C-7-d-1 — Use frame sync, TP4, for 64 x 64 element format.

p. 156, C-7-d-3 — Proper timing for the 64 x 64 element format is approximately 5 μs.

## APPENDIX III
## INTERCHANGE OF SCANNER SUB-ASSEMBLIES

The dual channel infrared scanner, as modified, can be used to scan two simultaneous images with either the original 40 x 40 element per frame format at 200 frames per second, or the new 64 x 64 element per frame format at 60 frames per second, by installing the corresponding scanner sub-assembly (consisting of motor, disc, sync projectors and detectors and associated mounting structure) and setting the two image format switches to the correct position. Instructions for interchanging the scanner sub-assemblies are given in this appendix.

### A. Sub-Assembly Removal

1. Remove the scanner rear cover and lower rear cover flange. (Scanner cover may be completely removed if desired for better visibility.)

2. Disconnect all accessable cables from the scanner Sub-Assembly (remove any cable clips as required and save them for re-installation). These include:

   a. J63 (motor power)
   b. J64 (6v. P.S.)
   c. J62 (det. power)
   d. P50 (line, frame, and disc sync)
   e. P52 (odd word sync)

3. Remove the following coaxial cables from the front panel bulkhead connectors:

   a. P1 (A channel video)
   b. P2 (B channel video)
   c. P4 (even word sync)
   (Remove cable clips as required.)

4. Disconnect the nitrogen line from the front panel bulkhead fitting.

5. Remove the 8 (¼ - 20 socket head) scanner sub-assembly mounting screws and slide sub-assembly back to gain access to remaining cables.

6. Remove cables (P57, P58, P59, P60, and P61) from the high voltage divider (and any others which may remain).

7. Clamp or bolt scanner baseplate to suitable support (unless already rigidly mounted) to prevent tipping and damage to scanner during Step 8.

8. Remove scanner sub-assembly by sliding it out the rear of of the scanner housing. (Note: See 7 above prior to removal.)

B. Transfer of Components to Other Sub-Assembly

Remove the following equipment from the scanner sub-assembly just removed and install it in the corresponding position on the other scanner sub-assembly:

1. All cables.

2. The nitrogen filters and associated mounting brackets and piping. (Note: Use extreme care when disconnecting nitrogen lines from detector cryostats to prevent damage. Do not allow cryostat to twist when disconnecting (or reconnecting) the line fittings or damage will surely result.)

3. 6 volt power supply and associated wiring.

4. High voltage power supply and associated wiring.

5. Infrared detectors.(with field lenses, narrow-band filters, and framing masks installed), Perry pre-amps, and associated wiring.

C. Optical System Changes

If interchange of the image splitting prism (installed) and the original image separators is also desired, this should be done while the scanner sub-assembly is removed.

1. Remove the image splitting prism by removing the base plate mounting screws.

2. Remove the two plane mirrors (inside halves of the image separator corner reflectors) from their storage locations on the two stepping motor mounting plates near the sides of the scanner and install them in their proper positions on the translation stages (see Fig. 38 of Ref. 1).

3. Remove the two translation stage stepping motor input cables from the storage clamps on the scanner side braces and connect them to the translation stage stepping motor input connectors.

4. Check optical alignment of installed reflectors (Step 2, above) and adjust as required using a helium-neon or other suitable alignment laser.

D. Sub-Assembly Installation

Installation of a scanner sub-assembly is accomplished, in general, by reversing the removal procedure given in paragraph A, above. In addition, attention should be given to the following details.

1. Make sure that the proper number of washers (1 lock washer and 2 flat washers) are used on each sub-assembly mounting bolt to prevent possible damage to the scanner mounting structure.

2. Before tightening the eight sub-assembly mounting bolts make sure that the scanner sub-assembly is

   a. centered (side-to-side) on the scanner baseplate,
   b. square with the baseplate (i.e., not rotated), and
   c. as far forward as possible without interference with the translation stage gearing or other components.

3. Since the sync lamp voltage is somewhat different for the two scanner sub-assemblies the 6-volt power supply (mounted on the sub-assembly baseplate) must be readjusted after interchanging the sub-assemblies. Nominal voltage settings are:

   + 5.8 volts for the 40 x 40 element format sub-assembly, and
   + 6.5 volts for the 64 x 64 element format subassembly.

   (see Chapter IV-B-4 for additional information).

4. The primary power input to the scanner motor (via P18 of the Scanner Control Unit, CU-2) must be changed when the scanner sub-assemblies are changed.

   120/208 v, 3-phase 400 Hz power is required for the 40 x 40 element format scanner sub-assembly, while
   120/208 v, 3-phase 60 Hz power is used with the 64 x 64 element format scanner sub-assembly.

5. The two image format switches must be set for the format to be used. One is located in the scanner on the lower edge of the relay panel, and the other on the console control unit chassis (near the right rear).

6. Following re-installation of the infrared detectors, they should be rotated for minimum hum pick-up (from the scanner motor primarily) prior to locking into final position. This is most easily accomplished by viewing the video output on an oscilloscope with the scanner operating and detectors warm. Note that it may be necessary to rotate the framing masks (after loosening the set screws holding them to the detector mounts) following rotation of the detectors for minimum hum (see also 7, below).

The detectors should be mounted as close to the scanning disc as possible without mechanical interference.

7. Framing adjustments (to achieve proper framing of the video image relative to the display unit raster) will normally be required following interchange of the scanner sub-assemblies. This is accomplished while viewing a "flood beam" infrared input to the scanner by means of adjustments to the framing mask (for each video channel) relative to the scanning disc.

   For the 64 x 64 element format sub-assembly, 3-axis vernier adjustments (vertical, horizontal, and rotation), with locking screws, are provided on each IR detector mount for this purpose. (The framing mask is mounted on the front of each IR detector.)

   For the original 40 x 40 element format sub-assembly separate (adjustable) framing masks mounted in front of the scanning disc were used. When re-installing this sub-assembly the original masks may be retained or the new detector mounted masks may be used alone, as desired. No vernier adjustments are provided on the original sub-assembly. Detector positioning is accomplished by loosening the three socket head screws holding the detector mount to the frame, positioning as required (permitted by the oversize mounting holes), and re-tightening the screws.

   Note that because of the infrared optical system used it is not possible to achieve perfect framing simultaneously for all three available magnifications (since the central image rays for the various magnifications arrive from slightly different directions, and since the framing mask cannot be located in exactly the same plane as the scanning disc). The best compromise for most purposes is obtained by making the framing adjustment using the median (X2) available magnification.

8. Since the data rates for the two image formats are somewhat different, the Miller code decoder center frequency controls (located behind the drop-down panel of the Miller code electronics chassis of the magnetic tape recorder) should be re-adjusted for minimum error rate during playback of recorded data from tape following interchange of the scanner sub-assemblies.

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